Toward Amp-Level Field Emission With Large-Area Arrays of Pt-Coated Self-Aligned Gated Nanoscale Tips

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***Abstract*— Design, fabrication, and characterization of Pt-coated, self-aligned, and gated Si field emission arrays are reported. Arrays of 320 000 tips with 10 μm pitch are employed to emit currents as high as 0.35 A (current density of 1.1 A/cm^2) at gate-emitter biases of 300 V. For reliability, the devices have a gate dielectric thicker than 2.5 μm maintaining the field inside gate insulator below 150 V/μm and a 5-nm-thick Pt-coating protecting the tips against sputtering by back-streaming ions. The Pt-coating also increases the capture cross section of electrons from the emitter cone, resulting in higher emission currents compared with uncoated Si tips when the supply of electrons is limited to the surface. The device failure at high currents is associated with plasma ignition due to local pressure rise caused by outgassing of the anode. At lower emission currents, the devices are capable of long-term emission (>3 h) at pressures as high as 10^{-5} Torr. Furthermore, a high-yield fabrication process is presented for large-area fabrication of highly-uniform gated tip arrays that could be expanded to active areas larger than 10 cm^2 to increase the emission current.**

***Index Terms*— Electron sources, field emission, gated tip arrays, self-aligned structures, vacuum electronic devices.**

I. Introduction

INTENSE high-current electron beams are needed for X-ray generation [1], pumping of gaseous lasers [2], and surface treatment of materials [3]. Vacuum electronic devices, such as gyrotrons [4], free electron lasers (FELs) [5], and terahertz vacuum electronic devices [6], [7] also employ high-current high-current-density electron beams. Electron sources operating based on field emission phenomenon [Fig. 1(a)] show great promise for these applications as these devices can produce current densities significantly higher than thermionic cathodes [8]–[16]. Field emission arrays (FEAs) have demonstrated emission at low voltages (<100 V) with current densities of 1–40 A/cm^2 [17]–[19]. State-of-the-art FEAs have produced currents as high as 300 mA at 15.4 A/cm^2 [19], [20]. Nevertheless, simultaneous high-current, high-current-density, long-term, and continuous emission have not been reported. The major challenges include low fabrication yield, nonuniform emission (leading to severe tip subutilization), and device failure due to gate dielectric breakdown, tip burn-out, and tip erosion due to sputtering by back-streaming ions.

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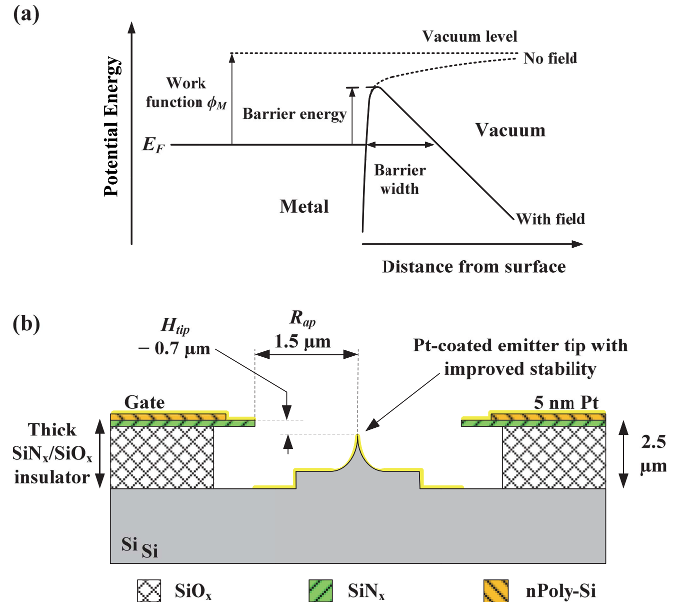

Fig. 1. (a) Potential energy diagram of electrons at the vicinity of metal surface w/wo normal electrostatic incident field. (b) Cross-sectional schematic of a self-aligned gated tip.

We have developed a high yield process with low process sensitivity for the fabrication of large-area self-aligned gated tip arrays with thick gate insulators for high current emission and improved reliability. Large arrays (320 000 tips) capable of emitting currents as high as 0.35 A at current densities of 1.1 A/cm^2 were fabricated. We report the design, fabrication, and characterization of Si FEAs, as well as failure mechanism at high currents.

II. Device Structure and Design

The schematic of the proposed field emission device is shown in Fig. 1(b). The device consists of a sharp tip

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surrounded by a proximal electrode, i.e., extraction gate. The electric field surrounding the tip is generated by applying a bias between the extraction gate and the emitter. A sharp emitter tip and the presence of a gate at close proximity are necessary to achieve field emission at low voltages. Moreover, the gate must be self-aligned, i.e., it must be located symmetrically around the emitter, to avoid off-axis electron emission, and to ensure that the emitted electrons are not intercepted by the gate (i.e., the field lines at the center of the tip, where the field and tunneling probability is maximum, do not terminate at the gate electrode). Our device comprises of a thick SiO_x/SiN_y gate dielectric stack (>2.5 μm) and a Pt-coated Si tip. A thick gate dielectric is necessary for reliable operation as the field in the dielectric must be a fraction of its breakdown field ($E_C \sim 1000$ V/μm). The Pt coating also improves resistance of the tips to corrosive gasses/ions.

Using elementary field emission theory, the emission current can be calculated from supply rate of electrons to the surface and the tunneling probability across the potential barrier [21], [22]. The emission current density J (A/cm^2) as a function of field at the surface of the tip F (V/cm), and the work function of tip material, ϕ (eV), can be approximated in [23] and [24]

$$J = a_{\mathrm{FN}} F^2 \exp\left(\frac{-b_{\mathrm{FN}}}{F}\right) \tag{1}$$

with

$$-a_{\mathrm{FN}} = \frac{A}{1.1\phi}\exp\left(\frac{10.4}{\phi^{1/2}}\right) \tag{2}$$

and

$$b_{\mathrm{FN}} = 0.95B\phi^{3/2} \tag{3}$$

where $A = 1.5 \times 10^{-6}$ and $B = 6.87 \times 10^7$. The terms 0.95 in (2) and 1.1 in (3) approximate the effect of the image term on field emission current. The field at each point on the surface of the emitter is a linear function of the applied gate-emitter voltage V_{GE}.

The gated tips were designed for emission currents above 1 μA at emitter gate voltages below 300 V. This ensures source current densities of higher than 1 A/cm^2 at tip-to-tip spacing as large as 10 μm. The critical design parameters [Fig. 1(b)] are the tip radius R_{tip}, gate aperture radius R_{ap}, and the height of the tip with respect to the gate plane H_{tip}. R_{tip} is mainly determined by the oxidation step used to sharpen the tips. The tips fabricated with our process have average radii less than 5 nm and the emitter cone angle is ~30° close to the tip as confirmed by SEM study. Assuming $R_{\mathrm{tip}} = 5$ nm and an emitter cone angle of 30°, electric field distribution in the device was simulated by COMSOL and the emission current from the tip was estimated by integrating (1) over the tip surface for devices with different values of H_{tip} and R_{ap}. For larger emitter cone angles, lower electrostatic fields and emission currents are expected [25]. These simulations neglect space charge effects [26], limitation in electron supply from the Si emitter cone, and the deviation of emission current from the classical Fowler–Nordheim (FN) behavior [27]. Although these effects will induce current variation as large as 2–3 orders of magnitude, at current densities below 10^7 A/cm^2 (2 μA/tip for our design) where the space charge effects are negligible, the error can be compensated by small change of the gate aperture and substrate conductivity.

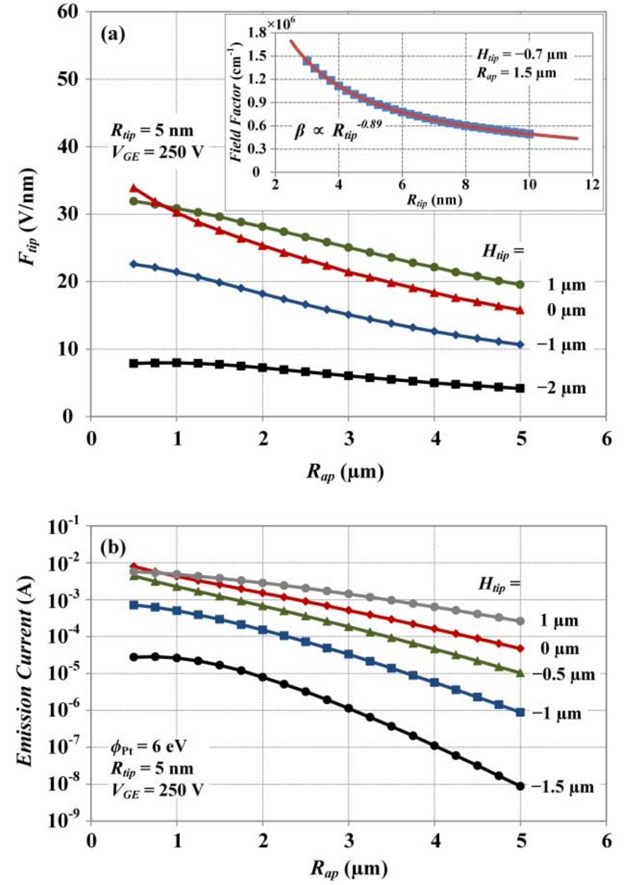

Fig. 2. (a) Simulated electric field at the tip and (b) calculated emission current per tip as a function of gate aperture radius R_{ap} for different tip height H_{tip} [Fig. 1(b)]. Negative H_{tip} values correspond to structures with tip below the gate plate. Inset of (a) shows the extracted field factor versus the tip radius R_{tip} for a fabricated device with $R_{\mathrm{ap}} = 1.5$ μm and $H_{\mathrm{tip}} = -0.7$ μm.

Fig. 2(a) shows the simulated electric field intensity at the tip as a function of R_{ap} at a V_{GE} of 250 V for devices with H_{tip} of -1 μm (tip below the gate plane) to 1 μm (tip above the gate plane). As expected, the electric field at the tip is higher for the devices with smaller R_{ap} and higher H_{tip}. The calculated current per tip is shown in Fig. 2(b) at V_{GE} of 250 V. Currents as high as 1 mA are predicted for tips close to the gate plane and R_{ap} of less than 1 μm. In practice, the emitted current will be less than predicted value from (1) due to a limitation in supply of electrons, resistive voltage drop from the surface to the bulk of the emitter, and heat generation that finally melts the tip. However, a tip with $R_{\mathrm{ap}} < 2$ μm located not more than 1 μm below the gate plane ($H_{\mathrm{tip}} > -1$ μm) should be capable of emitting currents >1 μA even if emitted current deviates from (1) by more than two orders of magnitude. FEAs with tips positioned 0.7 μm below the gate plane surrounded by gate electrodes with 3-μm apertures are considered in this paper as these devices can be fabricated with very high yields necessary for producing large FEAs. For this configuration, the simulated field factor (β) that

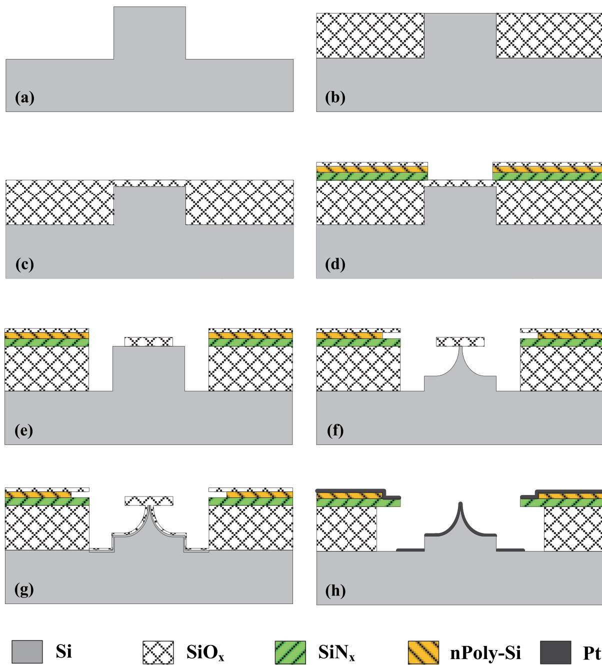

Fig. 3. Fabrication process flow of the proposed devices. (a) Si pillar etching. (b) SiO_x deposition and planarization. (c) Oxide growth. (d) Gate-stack deposition and via etching. (e) Gate and oxide cap definition. (f) Si isotropic etching. (g) Oxidation sharpening. (h) Oxide etching and Pt deposition.

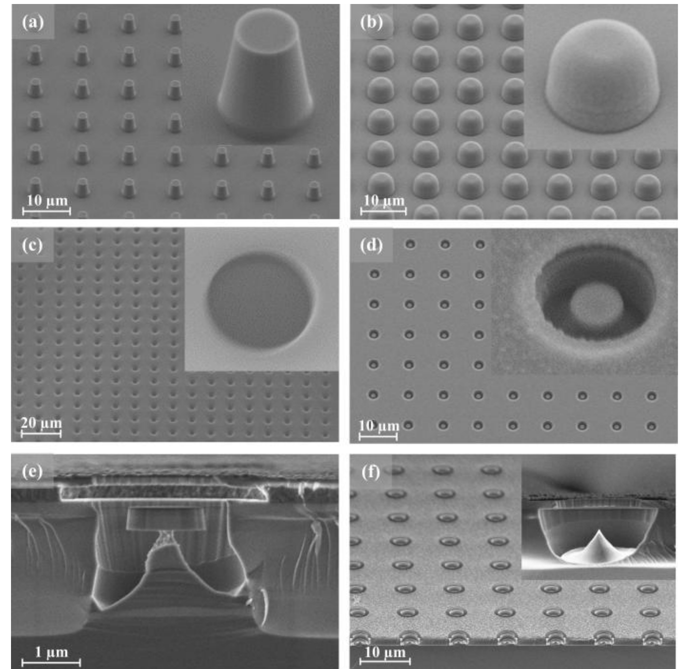

Fig. 4. SEM image of the device at different steps of the fabrication. (a) Pillar etching. (b) Oxide deposition. (c) Planarization. (d) Gate-stack etching. (e) Si isotropic etching. (f) Oxidation sharpening/oxide etching.

is the ratio of the electrostatic field at the tip (F_{tip}) to V_{GE}, is shown in the inset of Fig. 2(a) as a function of tip radius. This curve can be used to estimate the average tip radii using the field factor extracted from experimental results. The simulated field factor shows a $1/R_{\text{tip}}^{\alpha}$ dependence with $\alpha \sim 0.89$, which is consistent with [28] and [29].

III. Fabrication

A high-yield process was developed for fabricating gated tip arrays over large area substrates. The fabrication process, shown in Fig. 3, employs only three lithography steps to produce self-aligned gated tips. SEM images of the device at different steps of the fabrication are shown in Fig. 4. The fabrication begins with etching of 3-μm-tall pillars on 6-in n-type silicon substrates with resistivity of ~1–3 $\Omega \cdot$cm [Figs. 3(a) and 4(a)]. Dry etching of silicon is performed in HBr/Cl_2 plasma using a photoresist mask patterned in the first lithography step. The process conditions, such as pressure, plasma power, and gas flows have been optimized to produce a highly anisotropic etch profile with better than 85° sidewall angle. Formation of these pillars allows for deposition of a thick gate dielectric while the tips' positions are maintained close to the gate plane. Next, a 3-μm-thick SiO_x layer is deposited as the gate dielectric using plasma enhanced chemical vapor deposition (PECVD) method [Fig. 4(b)]. The sample is then annealed at 1000 °C for 3 h to improve the dielectric properties. Subsequently, the substrate is planarized to expose the Si pillars using a chemical mechanical polishing (CMP) process [Figs. 3(b) and 4(c)]. This is followed by thermal oxidation (0.2 μm) of the exposed Si regions to form the etch-stop layer for the anisotropic etching of Si that will be carried out to shape the tips [Fig. 3(c)]. To integrate the gate electrode, a stack of SiN_y (0.3 μm)/n-poly-Si (0.2 μm) is deposited by CVD technique and protected by a PECVD layer of SiO_x (0.2 μm). n-poly-Si is employed as the conductive layer for the gate electrode; while the SiN_y film serves as the top layer of the gate dielectric stack (SiO_x/SiN_y) for improved reliability as well as the mechanical support/shield layer for the gate electrode. In a second lithography step, an opening is patterned over the Si pillars in SiN_y/n-poly-Si/SiO_x stack [Fig. 3(d)]. The etching of SiN_y and n-Poly-Si is performed in SF_6/O_2 plasma while SiO_x is dry etched by CF_4/H_2 chemistry. Using the last lithography step, an oxide cap is defined over the Si pillars and the SiO_x/SiN_y/n-poly-Si/SiO_2 is simultaneously etched to form the gate electrode [Figs. 3(e) and 4(d)]. The gate opening ($\phi = 3$ μm) in the third mask is designed to be larger than the opening made by the second lithography in SiO_x/n-poly-Si/SiN_y stack ($\phi = 2$ μm) while the oxide cap pattern of the third mask has a diameter of 1 μm. Hence, the oxide cap that defines the tip is placed exactly at the center of the gate aperture. This ensures a self-aligned structure for the field emitters. However, alignment accuracy of better than ±0.5 μm is necessary for the oxide cap to be defined only over the pillars [Fig. 3(e)]. Later, an isotropic dry etching process [Figs. 3(f) and 4(e)] and oxidation sharpening [Fig. 3(g)] at low temperatures (<950 °C) shape the emitter tips [30]–[32]. At low temperatures, the rate of oxidation is mainly determined by stress build up (stress-retarded oxidation) rather than the oxidation time. As a result a uniform tip dimension is achieved over the large area since the oxidation at the tip is a self-limiting process. Previous studies show that the tips produced by this method have a lognormal distribution with standard deviation as low as 1 nm [28]. Finally, the oxide

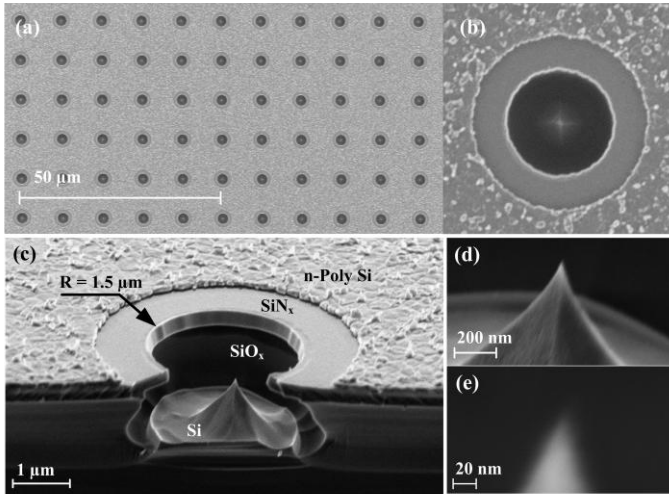

Fig. 5. SEM images of a fabricated array (320 000 tips in 0.32 cm^2) showing (a) and (b) top-view, (c) cross section, and (d) and (e) close-up images of a gated tip with 2.5-μm-thick gate dielectric and 3-μm gate aperture, confirming the self-aligned structure of the device and tip radius of <5 nm.

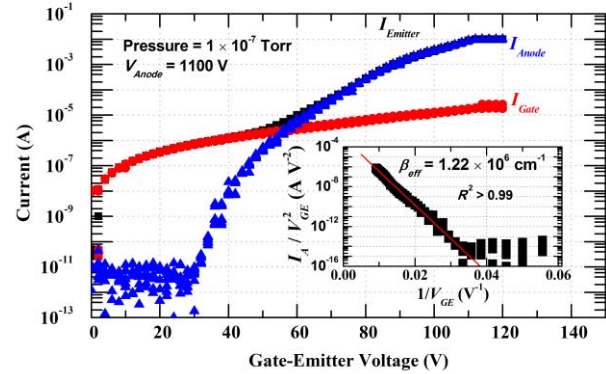

Fig. 6. Field emission characteristics of a fabricated array with 5-nm Pt-coating. Inset shows the FN plot of emission current indicating an average field factor of (1.22 ± 0.01) × 10^6 cm^{-1} and tip radii below 5 nm estimated from simulation results [Fig. 2(a)].

layer is wet etched through the gate aperture [Fig. 4(f)] and a thin layer of platinum (Pt) is e-beam deposited [Fig. 3(h)] to improve the gate conduction as well as to protect the tips and to increase the conductivity at the tip surface.

SEM images of a fabricated field emitter array composed of 320 000 tips in 0.32 cm^2 with 2.5-μm-thick gate dielectric, 3-μm gate apertures, and ∼5-nm tip radii are shown in Fig. 5. The SEM images shown in Fig. 5(a) and (b) confirm the devices are self-aligned. The top view images show that the tip (bright point in the image) is symmetrically surrounded by the gate electrode. The gate dielectric is composed of a SiO_x/SiN_y stacked layer similar to the devices in [33]–[35] for improved reliability. An overhanging SiN_y section is formed over the SiO_x layer after etching of the oxide grown for sharpening of the Si tips [Fig. 5(c)]. This SiN_y layer will serve as the shield layer for masking the sidewalls of SiO_x during the deposition of Pt layer. This prevents coating of the gate dielectric sidewall with Pt and reduces leakage current through the gate dielectric. The n-poly-Si layer does not extend to the edge of SiN_y layer since the dry etching of the SiN_y is not selective to n-poly-Si and n-poly-Si is oxidized during the oxidation sharpening step. However, the gate electrode is extended to the edge of the gate dielectric after Pt deposition. For the reported devices, the radius of gate aperture is 1.5 μm, the emitter tip is 0.7 μm below the gate plane, and the gate dielectric stack is thicker than 2.5 μm. The tips have radii below 5 nm, as shown in Fig. 5(d) and (e).

IV. Device Characteristics

A. Low-Current Emission

The transfer characteristics of a 320 000-tip array with 5-nm Pt-coating are shown in Fig. 6. The emission current was limited to 10 mA as the measurement was performed using Keithley SMU 237 units, which can supply/measure currents ≤10 mA in 0–1100 V bias range. A piece of Si mounted ∼2 mm above the device was used as the anode terminal. The gate and anode were biased at 0 and 1100 V, respectively, with a negative voltage applied to the emitter. The array emits 10-mA current at voltages below 120 V with better than 99% current transmission through the gate because of the self-aligned device configuration. The gate current is mainly attributed to leakage current through the gate dielectric rather than electron interception by the gate as similar gate currents was recorded under reverse gate-emitter voltages. Furthermore, the gate current does not increase linearly with the emitter current. The FN plot of the anode current is shown in the inset of Fig. 6. The anode current shows a linear FN behavior at V_{GE} voltages above 30 V where the emission current is higher than the noise floor. An effective field factor (β_{eff}) of (1.22 ± 0.01) × 10^6 cm^{-1} is calculated using (3) and the extracted slope from the linear part of the FN plot, assuming a linear field-potential relation. This suggests average tip radii of below 5 nm according to the simulation results [Fig. 2(a) inset], which is consistent with estimated tip radii from SEM images.

B. High-Current Emission

Emission characterization at high currents was conducted in pulse mode with less than 0.1% duty cycle using the experimental setup shown in Fig. 7(a). This is to avoid excessive pressure rise of the chamber that damages the FEA due to ion bombardment. Prior to the experiment, the chamber was baked at 180 °C for 24 h to outgas surface adsorbates. Nevertheless, a 10-mA continuous emission current raised the chamber pressure from the base pressure (∼1 × 10^{-9} Torr) to 10^{-7} Torr in less than 5 min. Measurements were performed with 100-μs pulses on the emitter with the anode biased at 1–3 kV and the gate connected to the ground. The emitter pulse was applied by a Glassman EQ1R1200 power supply controlled by a DEI PVX-4140 pulse generator while for anode bias a Glassman LH3R1.721 power supply was employed. The current of each terminal was calculated from the voltage drop across a known series resistor. The values of the resistors were confirmed by independent resistance measurement, and the voltage drops across the resistors were considered for reporting the *IV* characteristics. The substrate resistance from the emitter contact (backside of the substrate) to the emitting surface is estimated to be less than 5 Ω based on the device

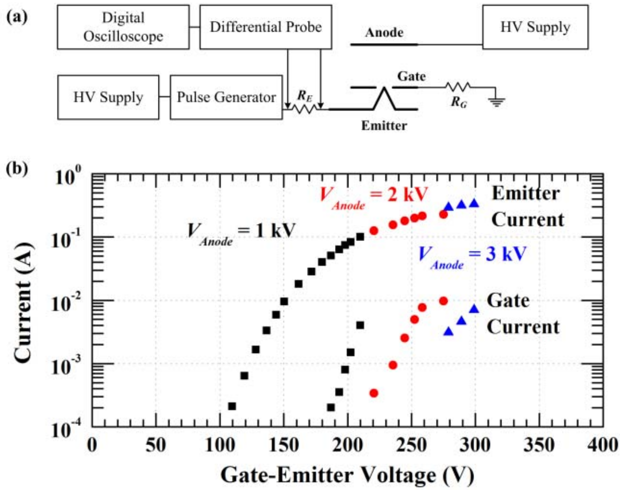

Fig. 7. (a) Experimental setup for high current measurements. (b) Field emission characteristics of a Ti/Pt-coated tip array. Currents as high as 0.35 A were emitted at gate-emitter voltage of 300 V. The average emitted current per tip increased from 250 nA for a Si tip to 1.1 μA for Ti/Pt-coated tip.

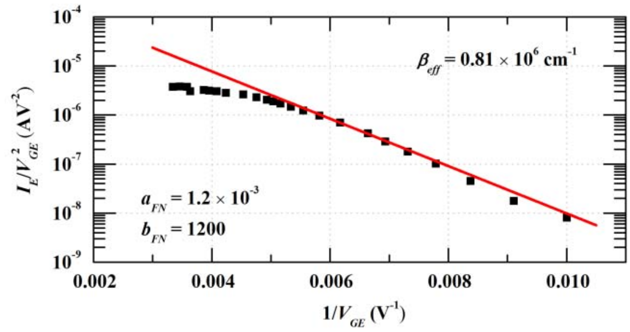

Fig. 8. FN plot of emission current for a Ti/Pt-coated array. Field factor of 0.81×10^6 cm^{-1} was obtained for the tips with a 40-nm-thick coating. Deviation of emission characteristics from FN behavior at high currents is associated with limitation in supply of the electrons from the substrate.

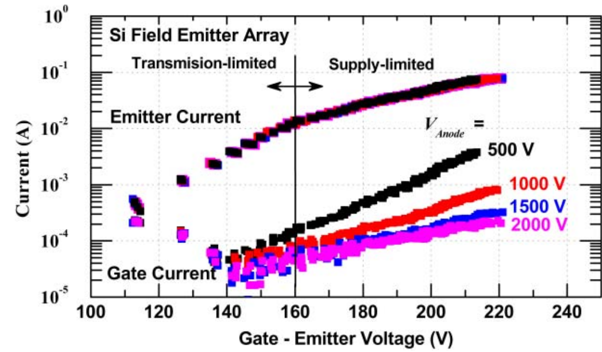

Fig. 9. Emission characteristics of a Si-tip array at different anode voltages; the emission current saturates at currents of ~250 nA/tip due to limitation in electron supply. Emitter current is independent of the anode voltage while gate current is reduced at higher anode voltages because of the stronger extraction field.

geometry and the substrate resistivity (1–3 $\Omega \cdot$cm). For the measurements, an array with a thicker coating (30-nm Ti/10-nm Pt) was used to reduce the resistivity and improve the current handling of the gate electrode. This was necessary as the device has a large gate-emitter capacitance of ~1 nF due to the large gate-electrode area (0.33 cm^2). Consequently, the transient current through the gate electrode can exceed 100 mA for 1 μs when gate-emitter voltage pulses higher than 100 V are applied through a series resistance of 1 kΩ. Using larger series resistors are not beneficial as they prolong the transient response of the device. On the other hand, a smaller series resistor increases the peak current through the gate and reduces the measurement accuracy because of lower voltage drop across the resistor.

Fig. 7(b) shows gate and emitter currents as a function of gate-emitter voltage for an array coated with Ti/Pt. This array produced currents as high as 0.35 A at V_{GE} of 300 V. The maximum current emitted by each tip was 1.1 μA, which resulted in 1.1 A/cm^2 for the fabricated array with 10-μm center-to-center tip spacing. The gate current rose faster than the emitter current at voltages above 150 V and higher anode voltages were needed to suppress the gate current. This can be explained by farther divergence of the electron beam at higher emission levels due to reduced extraction field and increased ratio of the transverse to vertical field for the electrons emitting off-axis. Consequently, a larger fraction of the beam is intercepted by the gate unless a stronger extraction field is applied.

Fig. 8 shows the FN plot of the emission current for the Ti/Pt-coated array. At voltages less than 200 V, the device exhibited a linear FN behavior with β_{eff} of 0.81×10^6 cm^{-1}. The array had a lower β_{eff} compared with the FEA with 5-nm Pt-coating (1.22×10^6 cm^{-1}) because of the larger radii of the tips with thicker coating layers. The deviation from FN characteristics at higher voltages (>200 V) is explained by electron supply limitation [32]. To validate this hypothesis, the emission characteristics of an uncoated Si FEA were measured. If there is no limitation in supply of electrons, at similar biases, Si FEAs are expected to emit higher currents compared with Ti/Pt-coated FEA because of the sharper emitting tips and the lower potential barrier height of Si (4.1 eV) compared with that of Pt (6 eV). Fig. 9 shows the terminal characteristics of a Si FEA. For this array, deviation from FN behavior was observed at lower currents of 20 mA corresponding to 60 nA per tip. Increasing the anode voltage did not affect the emission current, however, it significantly reduced the gate current due to the stronger extraction field.

C. Current Stability

Long-term performance of the Pt-coated FEAs was studied at different vacuum conditions. Fig. 10 shows the gate-emitter voltage and gate current as a function of time for a device continuously emitting 50 μA in high vacuum (~10^{-7} Torr). The device exhibited a steady emission voltage with less than 3 V of variations throughout the experiment. Operation at high vacuum also reduced the gate current over time. This can be attributed to reduction of the leakage current through the gate dielectric. Reduction of the gate leakage over time can be attributed to the complete filling of the defect states at the gate electrode/dielectric interface. Hence, the charge trapping rate declines over time as the carriers tunnel into farther defect states from the interface [36].

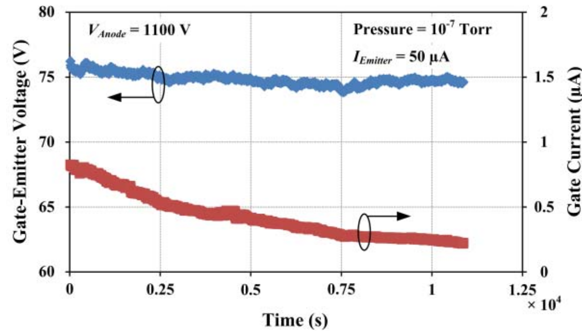

Fig. 10. Long-term characteristics of a Pt-coated FEA continuously emitting 50 μA in high vacuum (10^{-7} Torr). The emission voltage was stable during the experiment while the gate current decreased over time.

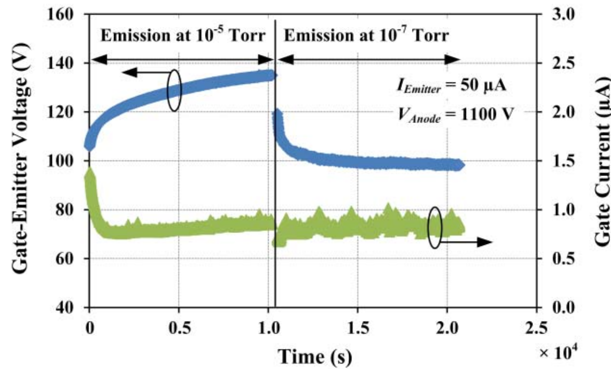

Fig. 11. Field emission at 10^{-5} Torr pressures: gate-emitter voltage (V_{GE}) and gate current over time for a device biased at constant emitter current of 50 μA. V_{GE} quickly returns to initial value after operating the device at 10^{-7} Torr. Variation in field emission characteristics points to reversible adsorption and desorption of particles over the Pt surface.

Long-term ($>10^4$ s) field emission in poor vacuum (10^{-5} Torr in N_2) was demonstrated for a constant emission current of 50 μA. Variation in terminal characteristics of the device during emission at poor vacuum followed by operation in high vacuum is shown in Fig. 11. Although, a gradual increase in V_{GE} voltage was necessary to maintain the current at a constant level, the original field emission characteristics were restored after operation in high vacuum ($\sim 10^{-7}$ Torr). The observed behavior of the FEA has been associated with the change in work function at the tip surface [9], [37]. This could be explained by reversible adsorption and desorption of gas molecules at the surface of Pt, verifying its role in protecting the tips.

D. Failure Mechanism at High Currents

Field emission at current levels above 50 mA was accompanied with sporadic current-overshoot events that eventually shorted the gate to emitter. During these events, usually accompanied by light emission, a large positive voltage was recorded on the gate even though a negative voltage pulse was applied to the emitter and the gate was connected to the ground through a resistor. This could be explained by formation of plasma between the anode and FEA, resulting in flow of a positive current from the gate to the ground supplied by the ions colliding with the gate. The plasma events are likely initiated by extensive outgassing of the anode due to heating or particle desorption caused by electron bombardment. This is supported by substantial pressure rise of the chamber even at low emission currents. Fig. 12(a) shows the chamber pressure over time when 10-mA current pulses with different pulse widths were emitted from FEA. The chamber pressure also increased linearly with emission current, as shown in Fig. 12(b).

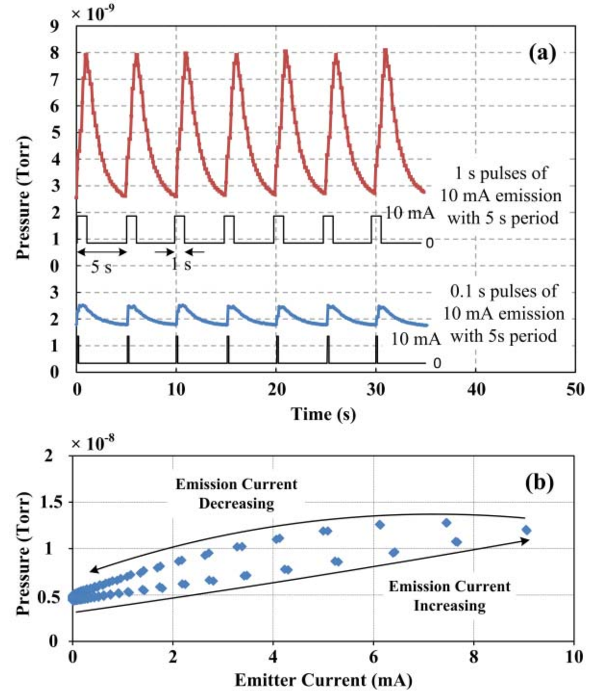

Fig. 12. (a) Pressure rise of the chamber due to 10-mA electron emission pulses with different pulse widths and (b) chamber pressure as a function of the continuous emission current. Extensive outgassing of the anode surfaces occurs at higher emission currents which results in plasma strike and prevents current emission higher than 0.35 A.

The hysteresis behavior observed in Fig. 12(b) could be attributed to the response lag between the temperature rise of the anode caused by energy deposition, desorption outgassing of gas molecules, and the transport of gas molecules to the pressure gauge and vacuum pump. The thermal capacity of the anode could also contribute to the time lag. It must be noted that the chamber pressure is measured $\sim$40 cm away from the device position in the chamber. As the flux of molecules is coming out of a volume of 0.2 cm^3, the local instantaneous pressure can be $10^6\times$ larger than the measured pressure on the inner walls of chamber since chamber volume is larger than 10^5 cm^2. Consequently, the local instantaneous pressure during emission can be at millitorr levels for a 50-mA emission current, which is sufficient to ignite plasma.

V. DISCUSSION

The physical processes governing field emission of the electrons are as follows: 1) transport from the emitter bulk to the surface; 2) transmission through the surface barrier; and 3) drift from the emitter surface to the anode. While the space charge limitation only affects drift of the emitted electrons to the anode, the supply of electrons to the emitter

surface is determined by electron density and velocity in the bulk. In our Pt-coated Si tips, the supply of electrons is limited by the Si substrate's carrier concentration; whereas, the onset of space charge current limitation is affected by work function of the surface, which in our case is ∼6.0 eV. Under this circumstance, we suggest that deviation of the current from FN behavior is more likely due to limitation in the supply of electrons from the bulk rather than the space charge effects.

The emission characteristics of the uncoated Si FEAs deviate from FN behavior at current levels above 20 mA. At such currents, each tip emits more than 60 nA if the emission is uniform across the array. This is in good agreement with the reported value of 100 nA for a Si tip in supply controlled region [32]. For a tip current of 60 nA, electrons enter from a surface area (capture cross section, $A_{\rm cc}$) of ∼370 nm^2 to the accumulation layer on the emitter surface. This capture cross section is based on an assumption that electrons are supplied from the bulk of the emitter with electron concentration n of $\sim 10^{16}$ cm^{-3} at saturation velocity $v_{\rm sat}$ of 10^7 cm/s according to $I = qn \cdot v_{\rm sat} \cdot A_{\rm cc}$. As the capture cross section is larger than the tip surface, the electric field has to penetrate into the Si to be able to sustain the current density. Assuming the electrons are supplied from the base of the emitter cone with height of z, $A_{\rm cc} = \pi \cdot z^2 \cdot \tan^2(\alpha_c/2)$, where α_c [∼30°, Fig. 5(e)] is the tip angle of the emitter cone. Based on this simplistic approach, for $A_{\rm cc}$ of 370 nm^2, the electrons are supplied from the emitter cone with >40-nm height, i.e., field must penetrate 40 nm into the silicon. At larger currents, the electric field must penetrate even deeper to enlarge the capture cross section. The field penetration into the emitter cone induces a potential drop between the substrate and the tip; hence, the emission current exhibits a saturating behavior with voltage [38].

Depositing a thin layer of metal over the emitter surface significantly increases the current capture cross section as electrons can enter the metal layer from a larger emitter cone area and move to the tip inside the metal. Indeed, the nonlinear FN behavior of the emission current for Pt-coated tips appeared at currents higher than 100 mA (∼300 nA/tip). This suggests a 5× increase in the capture cross section of the electrons. A thicker Pt coating cannot be used as it increases the tips' radii, which results in a lower field factor and reduced emission current. Current limitation due to low electron supply can be avoided by employing Si substrates with higher doping levels. Although this method is effective, if a very high doping concentration is used, the current rises to levels that damage the tip by excessive heating. Based on simulation results, the thermal current limit is in the range of 20 μA for a tip with 30° cone angle [similar to the tip fabricated here; see Fig. 5(e)]. Consequently, the doping concentration of substrate must be less than 10^{18} cm^{-3} to limit the current to below 10 μA and avoid tip burn-out. The drawback of this approach is the increased potential variation across the beam cross section and consequently higher beam emittance.

The fabrication method presented in this paper could be employed for producing large-area arrays (>10 cm^2) to increase the emission current. Our fabrication approach tolerates a wide variation in the CMP step compared with the methods employing CMP for defining the gate aperture [25], [39]. In those approaches, if there are nonuniformities in the thicknesses of the gate-stack or in the planarization process, the gate aperture will not be defined uniformly across the array. Consequently, there will be a large variation in current density of different tips that can result in severe subutilization of the array. According to our simulations, a 0.1 μm variation in the radius of aperture from 1.5 μm results in more than 50% change in emission current. More importantly, in extreme cases where the apertures are not opened or some of the tips are damaged, the intercepted current by gate increases or the emission current drops. However, in our approach, the aperture size is defined by lithography and etching performed after the planarization step. Hence, the CMP step does not affect the gate aperture dimensions and it can be continued until a planar surface is achieved over the entire wafer and Si posts surfaces. Moreover, only a single CMP step is required for defining a gate insulator with a thickness independent of the gate aperture size. Compared with the Spindt process [40], [41], there is no need for a directional deposition step with a grazing angle of incident. Furthermore, a thick gate dielectric can be employed without forming a post in the cavity or multiple deposition of the sacrificial and emitter material necessary for raising the tip position. Although the reported results in each graph have been obtained from a single device, the variation in effective field factor is less than 20% for more than five devices studied for each category of the emitters, i.e., Si, Pt-coated, and TiPt-coated FEAs.

VI. Conclusion

Emission currents as high as 0.35 A at current densities of 1.1 A/cm^2 were produced by an array of 320 000 tips in 0.32 cm^2 at gate-emitter voltages of 300 V corresponding to 1.1 μA/tip. The device has a self-aligned configuration for maximum electron extraction and a 2.5-μm-thick gate dielectric for reliability. The electrostatic field in the gate dielectric was maintained below 150 V/μm to ensure long-term operation. Device failure at high emission currents was attributed to plasma ignition due to excessive outgassing of the anode. At low pressures, long-term (∼3 h) operation was not only possible but also lowered emission voltage and gate current. Furthermore, the fabrication method presented here could be extended to larger areas (larger arrays) to obtain continuous emission currents >1 A.

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