Uniform High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Controlled by Vertical Si Ungated FETs—Part 1: Device Design and Simulation

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***Abstract*—In this paper, we report the design and simulation of electron sources composed of arrays of Si field emitters (FEs) that are individually ballasted by a current source. Each FE is fabricated on top of a vertical ungated field-effect transistor (FET), a two-terminal device based on a very-high-aspect-ratio Si column. The ungated FET takes advantage of the velocity saturation of electrons in silicon, the high aspect ratio of the ungated FET, and the doping concentration of the semiconductor to achieve current-source-like behavior. The proposed technology can be used to implement cathodes capable of reliable uniform and high current emission.**

***Index Terms*—Ballasting, cathodes, electron supply control, Si field emission arrays (FEAs), vertical ungated Si field-effect transistors (FETs).**

I. Introduction

MOST commercially available electron sources are based on thermionic emission in which electrons are "boiled" off the surface of metals or semiconductors when the thermal energy of the electrons is sufficient to overcome the potential barrier holding the electrons within the material [1]. Even though thermionic cathode technology has been quite successful, thermionic-based cathodes require high vacuum (pressure $< 10^{-5}$ torr) and high temperature (> 1250 K) to operate, which results in inefficient power consumption and portability constraints. The demand for more efficient electron sources has driven the research of cold cathode technologies, particularly field emission. Field emission arrays (FEAs) are potential cold cathodes that could be used in a variety of vacuum microelectronic and nanoelectronic device applications such as field emission displays (FEDs), high-frequency amplifiers, gas ionizers, X-ray sources, and multielectron beam lithography [2]–[7]. In the majority of these applications current level, stability, reliability, lifetime, and emission uniformity are the key metrics for cathode performance.

Field emission of electrons from metal or semiconductor surfaces consists of the following two processes: 1) *transmission of electrons* (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by the application of a high electrostatic field [8] and 2) *supply of electrons* from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the field emitter (FE). The typical field emission triode consists of a sharp tip located (centered) within a proximal gate electrode aperture (i.e., gate) and a third electrode (i.e., anode) facing the gate. Quantum tunneling of electrons to vacuum occurs when the bias voltage between the emitter and the gate generates a large enough electrostatic field on the surface of the tip ($> 3 \times 10^7$ V $\cdot$ cm^{-1}). The Fowler–Nordheim (FN) equation relates the current density to the electrostatic field and the work function [8], [9]. $I_E(V_{\rm GE})$, i.e., the current emitted from a tip biased at a voltage $V_{\rm GE}$ with respect to the gate (the emitter potential is negative with respect to the gate potential) is [10]

$$I_E(V_{\rm GE}) = \alpha_{\rm tip}\frac{A_{\rm FN}}{\phi t^2(y)}\cdot E^2_{\rm local}(V_{\rm GE})\exp\left[\frac{-B_{\rm FN}\cdot\phi^{3/2}}{E_{\rm local}(V_{\rm GE})}v(y)\right] \quad \text{(in amperes)} \quad (1)$$

where $\alpha_{\rm tip}$ (in square centimeters) is the emitting area of the tip, ϕ (in electronvolts) is the workfunction of the tip, $E_{\rm local}(V_{\rm GE})$ (in volts per centimeter) is the local electrostatic field at the emitter tip, $A_{\rm FN} = q^3/(8\pi h)$, and $B_{\rm FN} = (8\pi/3)/(\sqrt{2m}/qh)$, where q is the electronic charge, h is Plank's constant, and m is the electron's effective mass, and $t(y)$ and $v(y)$ are the Nordheim elliptic functions where $y = \sqrt{q^3E_{\rm local}/4\pi\varepsilon_o\phi^2}$ and ε_o is the electrical permittivity of free space. The Nordheim elliptic functions can be approximated as $t(y) = 1.1$ and $v(y) = 0.95 - y^2$ [11]. The local electric field is related to the applied

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voltage V_{GE} through $E_{\mathrm{local}}(V_{\mathrm{GE}}) = \beta \cdot V_{\mathrm{GE}}$ where β (in units per centimeter) is the field factor. Therefore, if we also assume that the emitter is at low temperature and it is made of a material with high electrical conductivity, (1) can be rewritten as

$$I_E(V_{\mathrm{GE}}) = \alpha_{\mathrm{tip}} \frac{1.27 \times 10^{-6}}{\phi} \cdot \exp\left[\frac{9.87}{\sqrt{\phi}}\right] \cdot \beta^2 \cdot V_{\mathrm{GE}}^2 \cdot \exp\left[-\frac{6.53 \times 10^7 \cdot \phi^{3/2}}{\beta \cdot V_{\mathrm{GE}}}\right] \text{ (in amperes)} \quad (2)$$

The field factor β relates the bias voltage to the surface electrostatic field and it is to first order equal to the inverse of the tip radius r. A better estimate of the field factor of a sharp FE with proximal gate (i.e., an emitter with tip radii far smaller than the other dimensions of the emitter, and with gate-to-substrate separation of the order of the emitter height) is given by [12]–[15]

$$\beta = \frac{k_F}{r^n} \text{ (in units per centimeter)} \quad (3)$$

where $k_F \approx 2.5 \times 10^6$, $n \approx 0.69-0.8$, and r (in nanometers) is the tip radius.

Control of the transmission process to produce high uniform current from FEAs has largely been unsuccessful due to the physics of the field emission process. Due to the exponential dependence on the field factor and, hence, the tip radius, emission currents are extremely sensitive to tip radii variation. Unfortunately, nanometer-sized tip radii in FEAs have a distribution with long tails such as Gaussian, lognormal, or Poisson [15]–[18]. Therefore, spatial variation of the tip radius results in spatial variation of the emission current and, hence, the current density. It also results in nonuniform turn-on voltages even for tips that are located next to each other. Fig. 1 is a semilog plot depicting a family of current–voltage (I–V) characteristics from a single tip for an FEA that has a tip radii distribution with average radius r_o and radius variation Δ_r. Each emitter current falls within the turn-on limit (controlled by the noise floor) and the burnout limit (due to Joule heating). For a constant bias voltage only a small fraction of the FEs in the array emits electrons because the sharper tips burn out early, before the duller tips emit, resulting in underutilization of the FEA. Attempts to increase the emission current by increasing the voltage often result in emitter burnout and shifting of the operating voltage to higher voltages. Even though burning out of the sharper tips of the FEA results in less emitter size variation and, hence, better emission uniformity, the larger average tip radius requires a larger bias voltage to produce the same current.

Consequently, alternative approaches for achieving uniform emission from FEAs have focused on control of the supply of electrons to the surface. In a metal, the supply of electrons is very high, making the control of the supply challenging. However, in a semiconductor, where the local doping level and the local potential determine the concentration of electrons, it is possible to configure the emitter such that either the supply process or the transmission process determines the emission current. Researchers have reported arrays of FEs individually ballasted using diodes operated in reverse bias mode [19]. In this approach, a p-semiconductor is used as base material, and

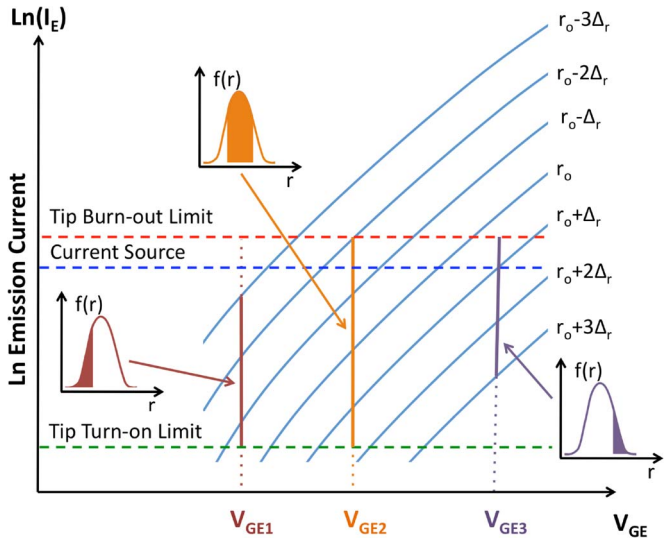

Fig. 1. Semilog plot of the family of I–V characteristics from a single tip for an FEA that has a tip radii distribution with average radius r_o and radius variation Δ_r. For a constant bias voltage, only a small fraction of the tip array emits current.

a p–n diode is created on each FE, either by ion implantation [20], or by using as emitters p-semiconductor tips that generate a depletion layer due to the high electrostatic field at the emitter surface [21]. The diode technology has demonstrated current control in FEAs. However, this approach poses technical challenges for implementing high current cathodes due to the magnitude of the saturation current of a diode in reverse bias. Also, researchers have reported that adjacent emitters compete for the supply of electrons, presumably because electrons in a p-Si substrate are scarce. As a consequence, for a given bias voltage, FEAs with a certain emitter pitch produce less current per emitter than FEAs with larger emitter pitch, visibly reducing the impact of emitter multiplexing for increasing the overall emission current [20].

Emission uniformity by controlling the supply of electrons to groups of emitters using ungated field-effect transistors (FETs) or MOSFETs as ballasting elements have been reported in the literature [22], [23]. However, these approaches are not ideal because emission nonuniformity would still occur within the subset of emitters controlled by the same ballasting element. Individual control of the supply of electrons to each emitter would prevent destructive emission from the sharper tips while allowing higher overall current emission because of the emission of duller tips. Ballasting of individual emitters using transistors has not been attempted before due to fabrication complexity. Furthermore, individual ballasting of Si emitters using classical MOSFETs results in small density of emitters per unit of area.

We recently proposed the use of vertical ungated FETs to individually control the emission of Si or CNT FEs in an array to achieve uniform and high current [24]. This paper further explores the proposed technology by providing a comprehensive analytical background. Section II introduces the idea of individually ballasting FEs with ungated FETs and presents a sensitivity analysis as metric for evaluating the effectiveness of this approach to achieve uniform emission. Section III reports the fabrication process and device simulations of the

ungated FET and the design of the individually ballasted FEs. Section IV discusses the results of the simulations. Finally, Section V summarizes the findings.

II. Individual Ballasting of FEAs

A. *Ballasting Using Linear Resistors Versus* FETs

The conventional approach to attain uniform electron emission from arrays of FEs has been through the use of large feedback resistors in series with the FEs [25]. However, this approach is unattractive because low spatial current spread is achieved at the expense of the current level, as shown in Fig. 2(a). A device that has current-source-like behavior would be able to simultaneously provide high current and high dynamic resistance, making it an ideal ballasting element to implement spatially uniform FEAs. The ungated FETs act as current sources, effectively providing high current with high dynamic resistance for drain-to-source voltages $V_{\rm DS}$ (voltage drop across the ungated FET) larger than the saturation voltage, as shown in Fig. 2(b) [26], [27]. I_D, i.e., the current through an ungated FET depends on the carrier concentration n, the electronic charge q, the drift carrier velocity v_d, and the cross-sectional area of the device $A(y)$, which, in general, is a function of the position along the channel y due to the variation in the surface depletion layer when a drain-to-source voltage $V_{\rm DS}$ is applied. The drift velocity is a function of the mobility μ and the electric field E_y, which is a derivative of the channel potential V_c. Therefore, the drain current I_D of the ungated FET is

$$I_D = A(y) \cdot q \cdot n \cdot \mu \cdot \frac{dV_c}{dy} \text{ (in amperes)} \tag{4}$$

where the mobility μ is a function of E_y, the mobility at low fields μ_o, and the carrier saturation velocity $v_{\rm sat}$, i.e.,

$$\mu = \frac{\mu_o}{\sqrt{1 + \left(\frac{\mu_o}{v_{\rm sat}}\right)^2 \left(\frac{dV_c}{dy}\right)^2}} \text{ (in square centimeters per volt per second).} \tag{5}$$

The surface depletion layer increases from the source end to the drain end of the ungated FET; therefore, the channel cross-sectional area $A(y)$ decreases from the source end to the drain end. Since the carrier concentration is constant, conservation of charge implies that the electron velocity and, hence, the electrostatic field increases from the source to the drain. For a certain drain-to-source bias voltage $V_{\rm DSS}$, the channel will pinchoff while the carrier velocity will reach its saturation value $v_{\rm sat}$, resulting in a drain saturation current $I_{\rm DSS}$. If $V_{\rm DS}$ is further increased, the depletion layer, in essence, grows toward the source resulting in the reduction of the effective channel, typically termed channel length modulation. Consequently, there is a gradual increase in the drain current I_D with applied drain-to-source voltage beyond $V_{\rm DSS}$. This behavior can be modeled as a linear increase in the drain current for drain-to-source voltages beyond $V_{\rm DSS}$, i.e.,

$$\begin{aligned} I_D &\cong I_{\rm DSS}\left(1 + \lambda(V_{\rm DS} - V_{\rm DSS})\right) \\ &= I_{\rm DSS} + g_{\rm out}(V_{\rm DS} - V_{\rm DSS}) \text{ (in amperes)} \end{aligned} \tag{6}$$

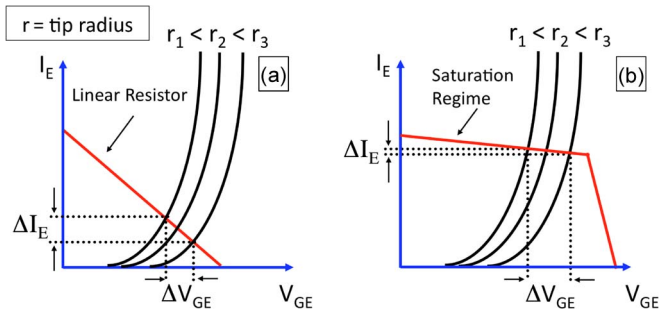

Fig. 2. Negative feedback of an FE using (a) a linear resistor and (b) an ungated FET. In the first case, low emission current variation within the FEA is achieved using a very large linear resistance, which results in low-current emission. If an ungated FET is used instead, both low variation and high-current emission are achieved because the current uniformity depends on the magnitude of the output resistance of the FET, which is to first order independent of its saturation current.

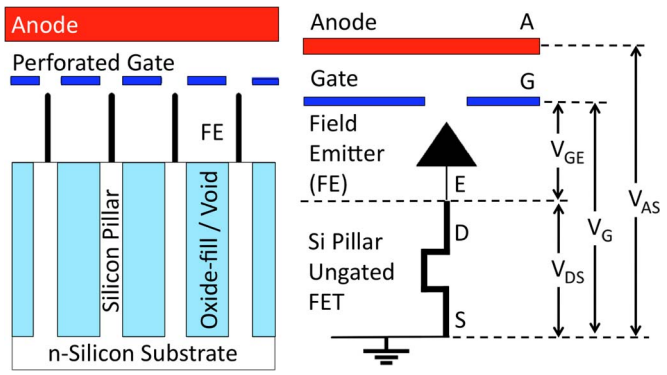

Fig. 3. (Left) Device structure. (Right) Equivalent circuit. Each FE is formed on top of a different silicon column (i.e., ungated FET). The bias voltage $V_{\rm GS} = V_G$ is divided between the voltage across the FE (i.e., $V_{\rm GE}$) and the voltage across the FET (i.e., $V_{\rm DS}$), i.e., $V_{\rm G} = V_{\rm GE} + V_{\rm DS}$.

where λ is the channel length modulation parameter, and $g_{\rm out}$ (in units per ohm) is the output conductance of the FET in the saturation regime. As shown in Section III, both high saturation current and high output resistance are achievable with the right combination of doping level N_D and device geometry. A high-aspect-ratio single-crystal Si column is a two-terminal ungated FET that can be fabricated using both deep reactive ion etching and thermal oxidation. The two-terminal vertical ungated FET can easily be integrated with FEAs to create dense arrays of individually ballasted FEs that emit spatially uniform high currents, as shown in Fig. 3. The FET acts as a current limiter of the FET/FE structure that is biased at a voltage V_G. For $V_{\rm DS} < V_{\rm DSS}$, the electric potential varies linearly along the length of the column, resulting in the column behaving similarly to a linear resistor. However, for $V_{\rm DS} > V_{\rm DSS}$ (Fig. 4), the channel is pinched off, and a depletion region forms at the drain end of the column. Increasing $V_{\rm DS}$ beyond this point causes the depletion region to extend, resulting in a reduction of the effective column length, analogous to channel length modulation in traditional MOSFETs. This change in effective column length ΔL results in the column behaving as if it were shorter, leading to a finite output conductance in the saturation regime. However, unlike in traditional MOSFETs, the channel pinch-off in a vertical ungated FET is a 3-D effect, as the extension of the depletion region varies on both orthogonal directions that are perpendicular to the FET source-to-drain axis.

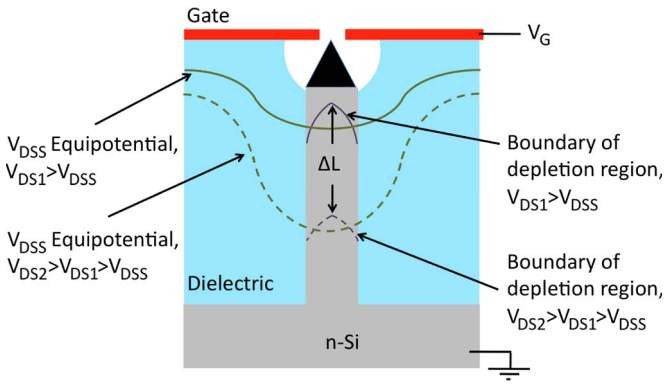

Fig. 4. Schematic diagram depicting the depletion region and equipotential lines for a single FET/FE.

B. Sensitivity Analysis

The sensitivity S is a measure of the emitter current variability across the array, and it is defined as the ratio of maximum emission current variation ΔI_E and the average emission current $\bar{I}_E$, i.e.,

$$S = \frac{\Delta I_E}{\bar{I}_E} = 2\frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}} \tag{7}$$

where $I_{\max}$ and $I_{\min}$ are the maximum and minimum emitter currents of the FEA, respectively. Examining (2), the current coming out of an FE has two independent sources of variability, namely: 1) the work function can vary due to absorption/desorption of gases and 2) the tip radius can vary across the emitter array. Therefore, the current sensitivity S of the FET/FE unit is defined in terms of the variations in the workfunction and the tip radius as

$$S = S_\phi + S_r = \frac{1}{I_E}\frac{\partial I_E}{\partial \phi}\Delta\phi + \frac{1}{I_E}\frac{\partial I_E}{\partial r}\Delta r \tag{8}$$

where S_ϕ and S_r are the current sensitivities with respect to the variations in the workfunction and the tip radius, and $\Delta\phi$ and Δr are the variations in workfunction and tip radius, respectively. In this discussion, we shall assume that temporal changes in the field-emitted current are due to temporal fluctuations in the workfunction (i.e., $\phi = \phi(t)$), and spatial nonuniformities in the field-emitted current are due to spatial variations of the tip radius (i.e., $r = r(\vec{R})$). Changes in the workfunction are mostly related to absorption/desorption of gases by the tip due to the presence of a background atmosphere. The typical workfunction variation in Si FEAs is 0.2 eV [23], which is less than 5% the nominal workfunction of silicon. The FET-based current regulation approach that we propose would be able to improve the temporal uniformity of each FE current down to a timescale of the order of the recombination time of carriers in silicon (∼1 ns). Tip radii spread across the array is originated in the tip fabrication variability, which could be worsened by long-term effects such as back ion bombardment of the emitter tips. The tip radii variation depends on the magnitude of the nominal tip radius: It can be as large as 86% for FEs with nanosized tip radii [15] and as low as 5% for FEs with one order of magnitude larger tip radii [28].

Although this work focuses on the nonuniformities in current emission due to spatial variation, the implementation of a FET-based individual electron supply control in an FEA can decrease both the temporal and spatial nonuniformities. Using (2) and (6), the emission current from a FET/FE unit is equal to the following implicit function:

$$I_E(V_G) = \alpha_{\text{tip}}\frac{1.27\times10^{-6}}{\phi}\cdot\beta^2\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})^2 \cdot \exp\left[\frac{9.87}{\sqrt{\phi}} - \frac{6.53\times10^7\cdot\phi^{3/2}}{\beta\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})}\right] \quad \text{(in amperes)} \tag{9}$$

where r_{out} is the output resistance of the FET. Using (3) and (9), the variation of the emitter current on the tip radius is given in (10), shown at the bottom of the page, and the variation of the emitter current on the workfunction is given in (11), shown at the bottom of the page. Based on this framework, we can obtain estimates of the radius-dependent sensitivity S_r and the workfunction-dependent sensitivity S_ϕ of an ungated FET/FE basic unit if we assume a set of operational parameters. Fig. 5 summarizes the simulation results. In these estimations, a total bias voltage V_G of 100 V was applied across the FET/FE unit, $\alpha_{\text{tip}} = 0.4\pi\cdot r^2$, $r_o = 30$ nm, $\phi = 4.5$ eV, $\Delta\phi = 0.2$ eV, $I_{\text{DSS}} = 1$ μA, and the output resistance was varied between 10^2 Ω and 10^{10} Ω. The simulation results show that the emission nonuniformity due to changes in the work function is visibly smaller than the emission nonuniformity due to tip radii spread across the FEA. Also, it is clear that FEAs with

$$\frac{dI_E}{dr} = -\frac{\frac{2n}{r} + \frac{6.53\times10^7\cdot\phi^{3/2}\cdot n\cdot r^{n-1}}{k_F\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})}}{\frac{1}{I} + \frac{2r_{\text{out}}}{(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})} + \frac{6.53\times10^7\cdot\phi^{3/2}\cdot r_{\text{out}}\cdot r^n}{k_F\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})^2}} \quad \text{(in amperes per centimeter)} \tag{10}$$

$$\frac{dI_E}{d\phi} = -\frac{\frac{1}{\phi} + \frac{4.93}{\phi^{3/2}} + \frac{9.8\times10^7\cdot\phi^{1/2}\cdot r^n}{k_F\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})}}{\frac{1}{I} + \frac{2r_{\text{out}}}{(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})} + \frac{6.53\times10^7\cdot\phi^{3/2}\cdot r_{\text{out}}\cdot r^n}{k_F\cdot(V_G - V_{\text{DSS}} - (I_E - I_{\text{DSS}})\cdot r_{\text{out}})^2}} \quad \text{(in amperes per electronvolt)} \tag{11}$$

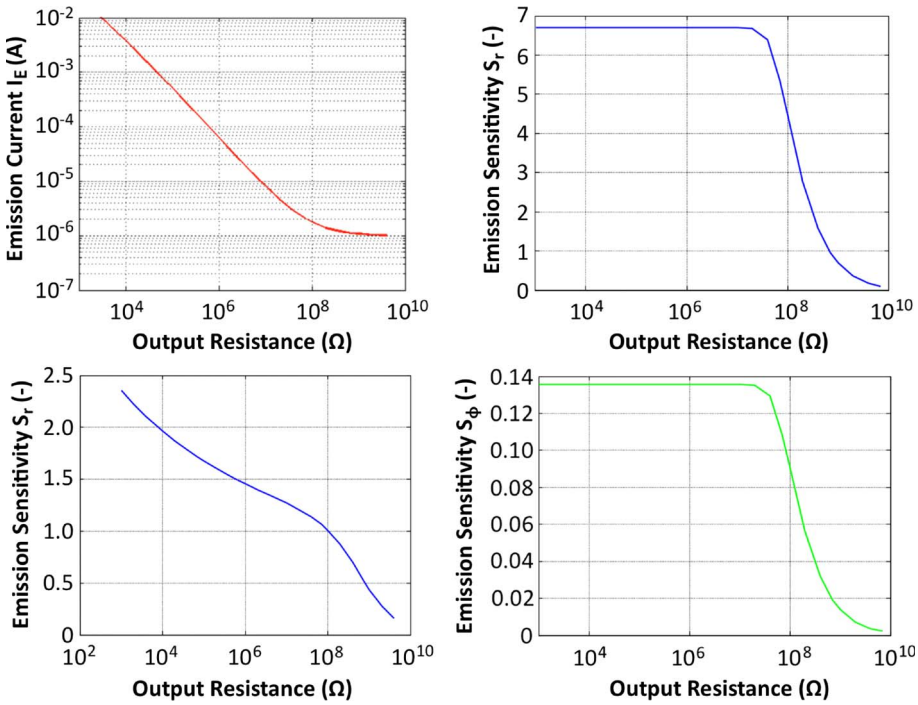

Fig. 5. (Top left) Emission current, (top right) S_r for $\Delta r = 5$ nm, (bottom left) S_r for $\Delta r = 1.5$ nm, and (bottom right) S_ϕ versus output resistance for an FET/FE unit with $r_o = 30$ nm, $\phi = 4.5$ eV, $\Delta\phi = 0.2$ eV, and $I_{\rm DSS} = 1$ μA.

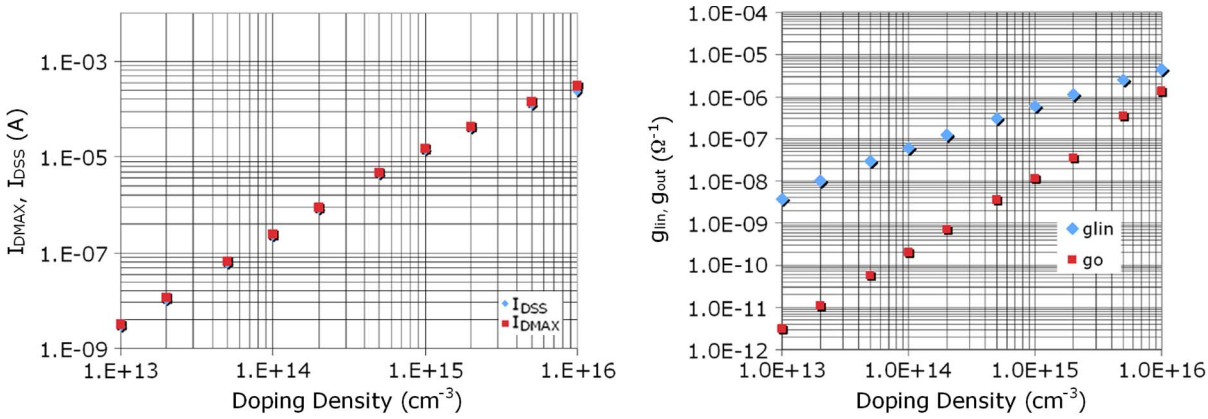

Fig. 6. (Left) Drain-to-source saturation current $I_{\rm DSS}$ and maximum current at 100 V $I_{\rm DMAX}$ and (right) linear conductance $g_{\rm lin}$ and output conductance $g_{\rm out}$ versus doping concentration for a 1 μm $\times$ 1 μm $\times$ 100 μm ungated Si FET.

smaller tip radii spread require less output resistance to achieve the same current regulation. For example if the output resistance of the FET is 100 MΩ, S_r is 4.5 if $\Delta r = 5$ nm (i.e., 16% r_o), while S_r is 1 if $\Delta r = 1.5$ nm (i.e., 4% r_o).

III. Ungated FET Process and Device Simulation

Extensive process and device simulations of high-aspect-ratio silicon columns were conducted using the SILVACO software (Silvaco International, Santa Clara, CA). The ungated FET cross-sectional area was set at 1 μm $\times$ 1 μm, while the channel length was varied between 10 and 100 μm and the doping concentration was varied between 10^{13} and 10^{16} cm^{-3}. From these simulations critical device parameters were extracted. Fig. 6 shows the maximum current at 100 V, saturation current, linear conductance, and output conductance as a function of the doping concentration N_D for a 1 μm $\times$ 1 μm $\times$ 100 μm ungated FET. We also explored the dependence of the linear resistance, output resistance, maximum current at 100 V, and saturation current on the channel length for an ungated FET with a fixed doping concentration and cross section. From Fig. 7, it can be inferred that the functional dependence of the linear and output resistance on the channel length is not the same (otherwise, the data would describe parallel lines in the plot); from the same figure, we can also infer that the FET has as a current-source-like behavior only when the aspect ratio of the FET is larger than about 50.

IV. Discussion

Fig. 8 illustrates the performance of the ungated FET/FEA structure and the ability of the FETs to increase the total output current of the FEA by protecting the sharper emitters from

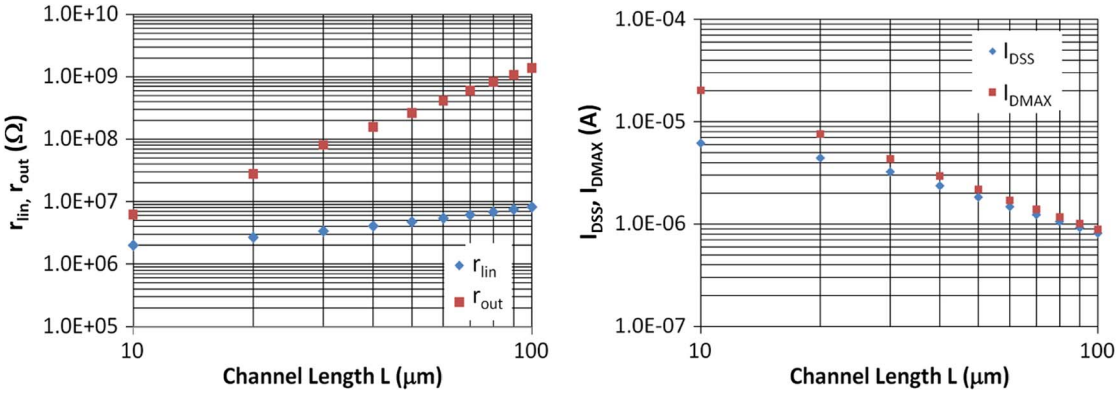

Fig. 7. (Left) Linear resistance $r_{\rm lin}$ and output resistance $r_{\rm out}$ and (right) drain-to-source saturation current $I_{\rm DSS}$ and maximum current at 100 V $I_{\rm DMAX}$ versus channel length for an ungated FET with 1 μm $\times$ 1 μm cross section and 2×10^{14} cm^{-3} doping concentration.

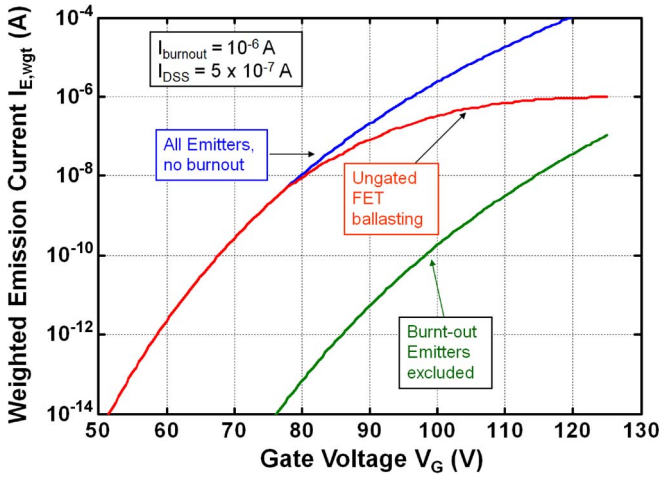

Fig. 8. Weighted I–V characteristics of an FET/FEA structure, weighted I–V characteristics of the FEA if no FETs are present and no emitter burnout occurs, and weighted I–V characteristics of the FEA if no FETs are present and emitter burnout occurs.

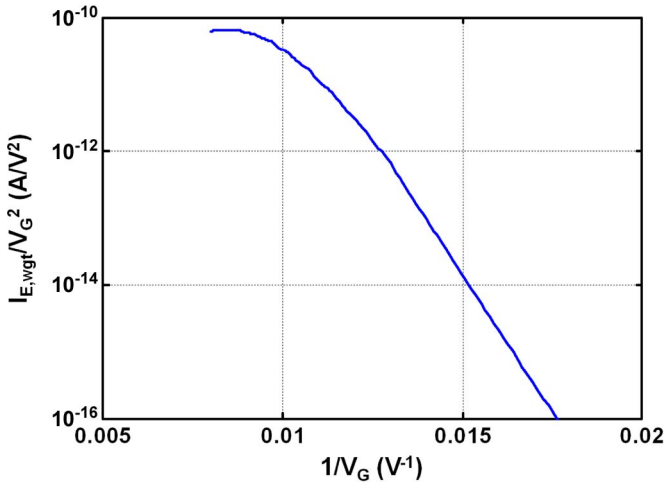

Fig. 9. For a low bias voltage, the weighted I–V characteristics of an individually ballasted FEA describe a straight line with negative slope in the FN plot. For large bias voltages, the current limitation by the FETs forces the slope of the FN plot to increase until it becomes horizontal. Further increase of the bias voltage will make the slope become positive.

burning out. For this simulation, it was assumed that the saturation current of the FET is 5×10^{-7} A, the burnout current is 1×10^{-6} A, and that the FEA is composed of FEs with tip radii that have Gaussian distribution with nominal tip radius 30 nm and standard deviation 5 nm. As seen in Fig. 8, for low bias voltages, the I–V characteristics of the FET/FEA structure is equivalent to the I–V characteristics of the FEA with no supply control structure. However, for large bias voltages, the weighted I–V characteristics of the FET/FEA structure saturates to a value close to the FET current saturation. A FEA biased at a voltage that produces current emission above the burnout value would lose a portion of its elements due to Joule heating. The net result of the burnout is a weighted I–V characteristics with a shift in the operational voltage and lower current emission for the same bias voltage. From (2), it can be inferred that the I–V characteristics of an electron source that obeys the FN model describe a straight line with negative slope in a FN plot, i.e., a plot of $\ln(I/V_G^2)$ versus V_G^{-1}. However, an individually ballasted FEA has a FN plot that for large enough bias voltages the slope increases until it becomes horizontal or even positive, as shown in Fig. 9. Based on the analysis and simulations presented in this section, we estimate that ungated FETs with substantially larger aspect ratios than the ones proposed by Takemura *et al.* [22] are required to achieve good spatial emission uniformity.

A potential drawback of the FEA that is individually ballasted by ungated FETs is the spread in energy of the emitted electrons. Energy spread results from the variation in the tip radius and, hence, the gate-to-emitter voltage required to obtain the particular emission current imposed by the current limiter. There are several approaches to mitigate against the spread in energy of the emitted electrons. One approach will be to operate the device at the space charge limit. Another approach would be to lower the operating voltage and, hence, the energy spread by scaling the tip radius and the gate aperture to smaller dimensions in order to increase the field factor β.

V. Summary and Conclusion

We have demonstrated through simulations that large arrays of Si FEs can achieve high and uniform electron current emission if each FE is individually controlled (ballasted) by an ungated FET. The ungated FET achieves current-source-like behavior due to the velocity saturation of carriers in silicon,

the very high aspect ratio of the ungated FET, and the doping concentration. We have proposed individually ballasted FEAs composed of FET/FE units where the FE is fabricated on top of a vertical ungated FET (a high-aspect-ratio silicon column) to maximize the FEA emitter density. The FET ballasting technology that we propose enables the implementation of high-current cathodes composed of massive and dense arrays of individually controlled FEs.

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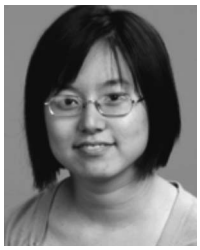

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