Uniform High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Controlled by Vertical Si Ungated FETs—Part 2: Device Fabrication and Characterization

Luis Fernando Velásquez-García, *Senior Member, IEEE*, Stephen A. Guerrera, *Student Member, IEEE*, Ying Niu, *Member, IEEE*, and Akintunde Ibitayo Akinwande, *Fellow, IEEE*

***Abstract*—We report the demonstration of electron sources that achieve high-current and uniform emission using dense arrays of Si field emitters (FEs) that are individually ballasted by a current source. Each FE is fabricated on top of a vertical ungated field-effect transistor (FET), a two-terminal device based on a very-high-aspect-ratio Si column. The ungated FET takes advantage of the velocity saturation of electrons in silicon, the high aspect ratio of the ungated FET, and the doping concentration to achieve current-source-like behavior to obtain reliable uniform and high-current electron emission. Emitted currents in excess of 0.48 A were demonstrated.**

***Index Terms*—Ballasting, cathodes, electron supply control, Si field emission arrays (FEAs), vertical ungated Si field-effect transistors (FETs).**

I. Introduction

FIELD emission cathodes are an attractive alternative to thermionic electron sources because they are less power hungry, potentially more reliable, faster, and more compatible with portable applications. Field emission arrays (FEAs) could be used in a variety of vacuum microelectronic and nanoelectronic device applications such as field emission displays (FEDs), high-frequency amplifiers, gas ionizers, X-ray sources, and multielectron beam lithography [1]–[6]. In the majority of these applications current level, stability, reliability, lifetime, and emission uniformity are the key metrics for cathode performance. Field emission of electrons from metal or semiconductor surfaces consists of the following two processes: 1) transmission of electrons (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by the application of a high electrostatic field and 2) supply of electrons from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the field emitter (FE). Control of the transmission process to produce high uniform current from FEAs has largely been unsuccessful because of the exponential dependence of field emission current on the emitter tip radius [7] and the long-tail distribution of nanosharp FE arrays [8]–[11]. Consequently, alternative approaches for achieving uniform emission from FEAs have focused on control of the supply of electrons to the surface. In a metal, the supply of electrons is very high, making the control of the supply challenging. However, in a semiconductor, where the local doping level and the local potential determine the concentration of electrons, it is possible to configure the emitter such that either the supply process or the transmission process determines the emission current. Emission uniformity by controlling the supply of electrons to groups of emitters using ungated field-effect transistors (FETs) or MOSFETs as ballasting elements has been reported in the literature [12], [13]. However, these approaches are not ideal because emission nonuniformity would still occur within the subset of emitters controlled by the same ballasting element. In addition, researchers have reported FEAs individually ballasted by linear resistors [14]. However, this approach is unattractive because low spatial current spread is achieved at the expense of the current level.

We recently proposed the use of vertical ungated FETs to individually control the emission of Si or CNT FEs in an array to achieve uniform and high current [15]. The ungated FET takes advantage of the carrier velocity saturation in silicon, the very high aspect ratio of the ungated FET, and the doping concentration to achieve current-source-like behavior. In part 1 of this paper, we showed through simulations that the control of electron emission from individual FEs using ungated FETs can span a wide range of emission current per tip and also achieve full current limitation of the FEA [16]. Here, we provide experimental proof that arrays of Si FEs individually

Manuscript received November 29, 2010; revised February 11, 2011; accepted February 20, 2011. Date of publication May 15, 2011; date of current version May 20, 2011. This work was supported in part by the Air Force Office of Scientific Research (program manager Ryan Umstadt and Robert Barker), by the Defense Advanced Research Projects Agency (DARPA)/Microsystems Technology Office (program manager Mark Rosker), and by the Army Research Office (Dev Palmer). The review of this paper was arranged by Editor W. L. Menninger.

L. F. Velásquez-García is with the Microsystems Technology Laboratories (MTL), Massachusetts Institute of Technology (MIT), Cambridge, MA 02139 USA (e-mail: lfvelasq@mit.edu).

S. A. Guerrera is with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

Y. Niu is with Integrated Defense Systems, Raytheon Corporation, Fort Wayne, IN 46808 USA.

A. I. Akinwande is with the Microsystems Technology Office, DARPA, Arlington, VA 22203 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2128323

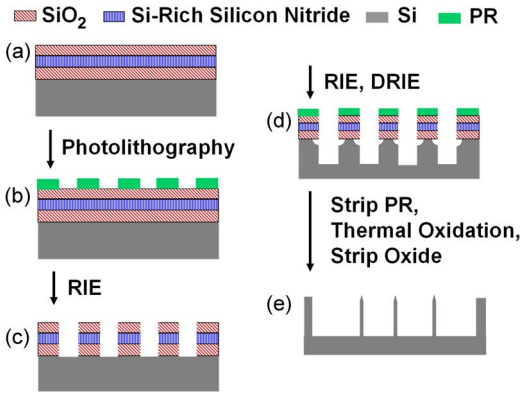


Fig. 1. Process flow to fabricate arrays of FEs individually controlled by vertical ungated FETs.

ballasted by vertical ungated FETs are capable of uniform and high electron current emission. Section II reports the fabrication of arrays of Si FEs that are individually controlled by a vertical ungated FET. Section III reports and analyzes the experimental data of the individually ballasted FEAs, clearly showing that the FETs control the current emission. Section IV discusses the results. Finally, Section V summarizes the findings.

II. Fabrication

Large arrays of FEs (10^6 emitters in 1 cm^2) that are individually controlled by vertical ungated FETs were fabricated to demonstrate large and uniform field emission currents. The fabricated devices have no integrated extraction gate and, hence, an external perforated grid provided the extraction field. The process flow to fabricate the arrays of FEs individually controlled with vertical ungated FETs uses 6-in n-Si wafers and is shown in Fig. 1, while Fig. 2 is a collage of SEMs at different stages of the fabrication. First, the substrates are coated with a thin-film stack (a 0.5-μm plasma-enhanced chemical-vapor-deposited SiO_2 film on top of a 0.5-μm low-pressure chemical-vapor-deposited silicon-rich silicon nitride film on top of a 0.5-μm thermal SiO_2 film). Then, the thin-film stack is etched using contact photolithography and reactive ion etching (RIE) to form arrays of 1000×1000 squares 3.5 μm wide spaced 10 μm. After that, an isotropic reactive ion etching step commences the FE sharpening. Next, the vertical ungated FETs are etched using deep RIE (DRIE) [Fig. 2(a)]. Finally, the wafers are RCA cleaned and oxidized to form massive arrays of nanosharp tips [Fig. 2(b)] on top of columns about $1 \times 1 \times 100$ μm [Fig. 2(c)].

III. Experimental Results

A. Individually Ballasted FEAs, DC Current–Voltage (I–V) Characteristics

We were able to obtain evidence of current limitation from arrays of Si FEs individually controlled by ungated FETs that were tested at high dc voltages in vacuum (10^{-9} torr). The characterization of large FEAs made of silicon with a doping concentration below 2×10^{14} cm^{-3} showed a substantial degree of electron supply control.

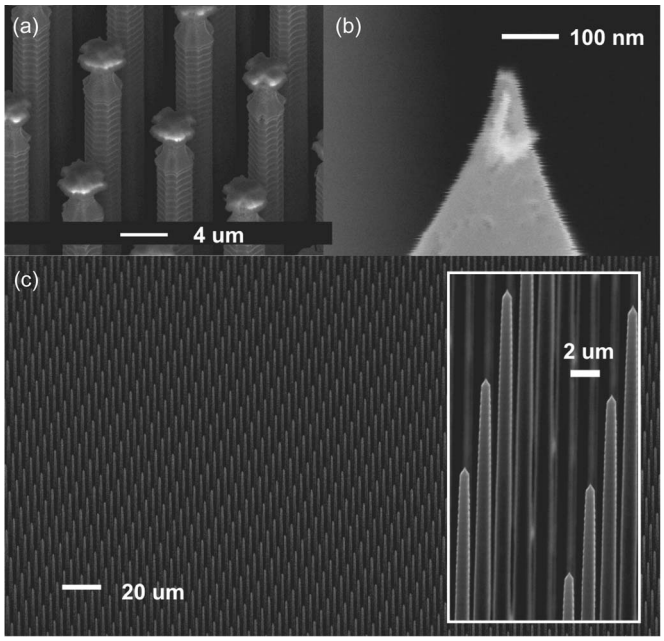


Fig. 2. Selected images of the process flow to fabricate individually ballasted FEAs using vertical ungated FETs: (a) DRIE of the vertical ungated FETs with partially sharpened Si FEs; (b) close up of an emitter tip after full sharpening; (c) field view of a large FEA and close up of the final FET/FE structure.

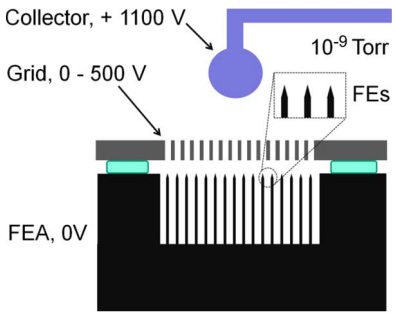


Fig. 3. Schematic of the triode setup used to test the individually ballasted FEAs. In the dc tests, the FEA, grid, and collector were energized using three Keithley 237s.

Experimental Setup: Arrays of one million Si FEs individually ballasted by vertical ungated FETs (1 cm^2 of emitting area) were fabricated as described in Section II using silicon wafers with resistivity values that span two orders of magnitude of doping concentration (10^{13}–10^{15} cm^{-3}). The FEAs were tested using the setup shown in Fig. 3. In the setup, a global unaligned perforated grid was placed in close proximity to the emitter tips using a thin ($\sim$25 μm thick) polymer gasket that acted as stand-off between the substrate and the grid. When a voltage is applied between the grid and the FEA, electrons are field emitted from the FEA and a fraction of which is transmitted through the transparent grid. There is a 2-mm-diameter metallic sphere suspended about 5 mm above the grid that was used as an external collector. The collector was biased at +1100 V. The objective of using a collector is to allow us to discriminate between leakage current through the dielectric and electron emission. If there is a linear dependence between the current collected by the grid (grid current I_G) and the current collected by the suspended electrode (collector current I_C), we

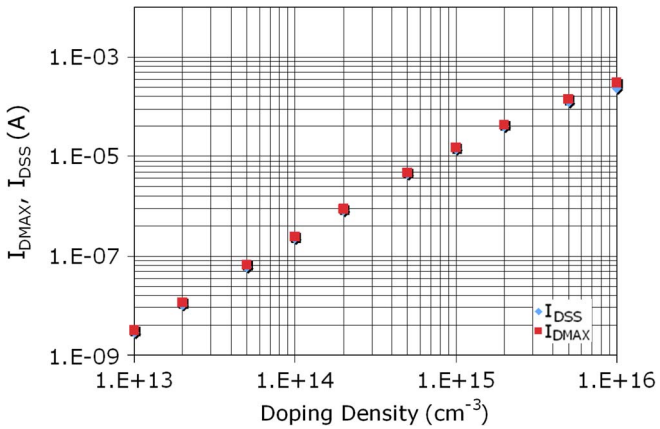


Fig. 4. Simulation estimates of the drain–source saturation current $I_{\rm DSS}$ and maximum current at 100 V $I_{\rm DMAX}$ versus doping concentration for a $1 \times 1 \times 100$ μm ungated Si FET.

can conclude that both currents have the same physical origin. Since the suspended electrode has no physical contact with the FEA, the origin of the measured currents cannot be leakage current through the polymer gasket. We also conducted reverse-polarity tests to verify that the measured current was field emitted, and we verified that the current emitted by the FEA (I_E) was equal to the grid current plus the collector current. Also, we conducted Fowler–Nordheim (FN) analysis of the data to verify that the FEA was the origin of the measured currents. We used a set of Keithley 237s controlled by Labview to collect the I–V characteristics of the arrays of FEs individually controlled by vertical ungated FETs. The instruments are able to measure a maximum current of 10 mA and apply a bias voltage between -1100 and $+1100$ V.

Highly Doped Substrates, Low Current: An FE individually controlled by an ungated FET is, in essence, a potential divider with the voltage applied between the grid and the ground, i.e., V_G, divided between the voltage drop between the grid and the FE, i.e., $V_{\rm GE}$, and the voltage drop between the drain and the source of the ungated FET, i.e., $V_{\rm DS}$. Emission current from a single FE that is individually ballasted will be limited when the voltage drop across the FET is such that the ungated FET is operating in its current saturation region, i.e., the drain-to-source voltage drop across the FET is greater than its corresponding saturation voltage $(V_{\rm DS} \geq V_{\rm DSS})$. The saturation current of a $1 \times 1 \times 100$ μm vertical ungated FET with a doping concentration of 1×10^{15} cm^{-3} is about 14 μA [16] (Fig. 4), while the maximum emission current that can be measured using the dc testing setup is 10 mA, which corresponds to 10 nA per tip if the emission is evenly distributed. Therefore, the I–V characteristics from an individually ballasted FEA made of highly doped silicon should show no deviation from the expected FN behavior. In this case, the current I_E from an FE due to a bias voltage V_G is given by the FN equation [7]:

$$I_E(V_G) = \alpha_{\rm tip} \frac{1.27 \times 10^{-6}}{\phi} \cdot \exp\left[\frac{9.87}{\sqrt{\phi}}\right] \cdot \beta^2 \cdot V_G^2 \cdot \exp\left[-\frac{6.53 \times 10^7 \cdot \phi^{3/2}}{\beta \cdot V_G}\right] \text{ (in amperes)} \quad (1)$$

where ϕ is the workfunction of the tip, $\alpha_{\rm tip}$ is the area of the tip involved in the emission, and β is the field factor of the tip. The field factor relates the electrostatic field at the surface of the tip to the bias voltage. A semiempirical expression to estimate β is [17]

$$\beta = \frac{k_F}{r^n} \text{ (in units per centimeter)} \quad (2)$$

where $k_F \approx 2.5 \times 10^6$, $n \approx 0.69-0.8$, and r (in nanometers) is the tip radius. Fig. 5(a) shows the I–V characteristics of a one-million FEA made of silicon with a doping concentration of about 1×10^{15} cm^{-3}. The device emits current above the noise floor for voltages larger than 125 V, and a maximum total emission current of about 100 μA. Fig. 5(b) clearly indicates a linear dependence between the collector current and the grid current (the collector current is about 2.4% the grid current with a correlation $R^2 > 0.995$), which suggests that the measured currents are field emitted. As shown in Fig. 5(c), the FN plots of the grid and collector currents are parallel lines with an average slope that corresponds to a field factor β of 2.34×10^5 cm^{-1} if a workfunction of 4.05 eV is assumed for Si. Using (2) with $k_F = 2.5 \times 10^6$ and $n = 0.69$ results in an estimated tip radius of about 31 nm. From Fig. 5(d), the typical tip radius from SEMs is about 51 nm. As expected, the tip radius from the FN plot is smaller than the typical tip radius from SEMs because only the sharper tips of the tail end of the FEA distribution are emitting.

Lowly Doped Substrates, Low Current: A large FEA emits low current most likely because the applied bias voltage is only able to turn on a few emitters of the array rather than because all the emitters are contributing to the emission. The emitters that are active will most likely have similar tip radii, resulting in a narrower tip size distribution and a similar behavior that could show a substantial deviation from the expected FN behavior before more emitters turn on and contribute to the total current output. We experimentally confirmed that even for relatively small current levels ($<$ 1 mA), individually ballasted FEAs made with lowly doped silicon exhibit I–V characteristics that show a substantial degree of electron supply control. For example, Fig. 6(a) shows the I–V characteristics of a one-million FEA made of silicon with a doping concentration of about 2×10^{13} cm^{-3}. The device emits current above the noise floor for voltages larger than 200 V, and a maximum total emission current of about 145 μA was measured. Fig. 6(b) clearly indicates a linear dependence between the collector current and the grid current (the collector current is about 1% the grid current with a correlation $R^2 > 0.995$), which suggests that the measured currents are field emitted. As shown in Fig. 6(c), the FN plots of the grid and collector currents at low voltage are two parallel straight lines with negative slope. However, for voltages above 575 V, the FN plots clearly show an increase of the slope (i.e., the slope becomes less negative) due to the current regulation of the FETs. Using the slope of the linear part of the FN plots, we estimate a field factor β of 1.3×10^5 cm^{-1} using 4.05 eV as the workfunction for Si. Using (2) with $k_F = 2.5 \times 10^6$ and $n = 0.69$ results in an estimated tip radius of about 72.5 nm. From Fig. 6(d), the average tip

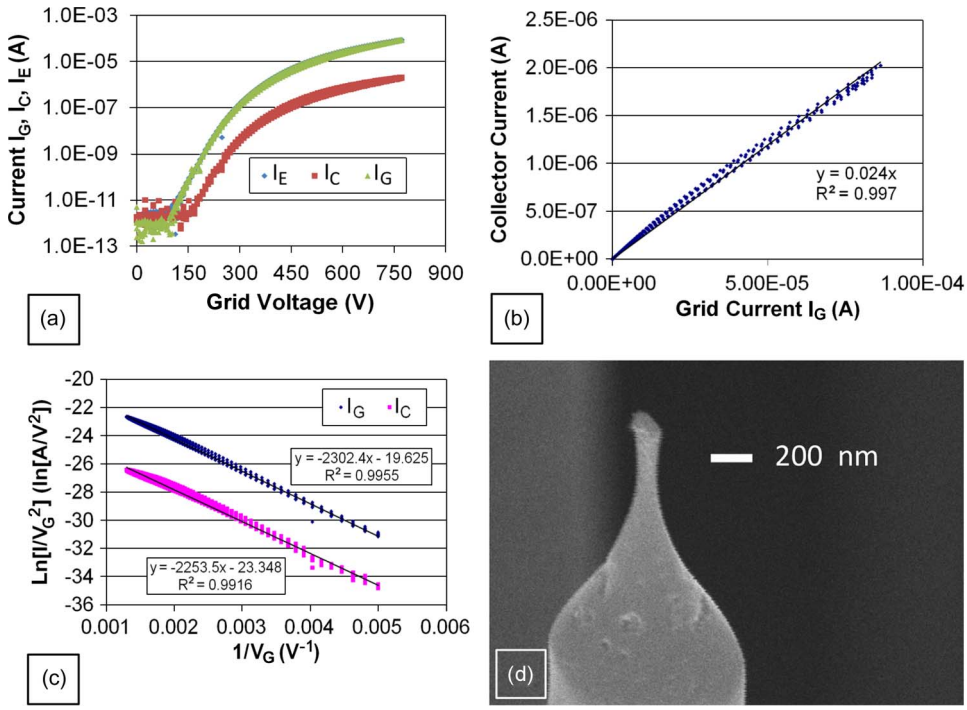


Fig. 5. Characterization of a one-million array of FEs individually controlled by ungated FETs made with highly doped silicon: (a) I–V characteristics; (b) collector current versus grid current; (c) FN plot of the grid current and collector current; and (d) SEM of a typical FE.

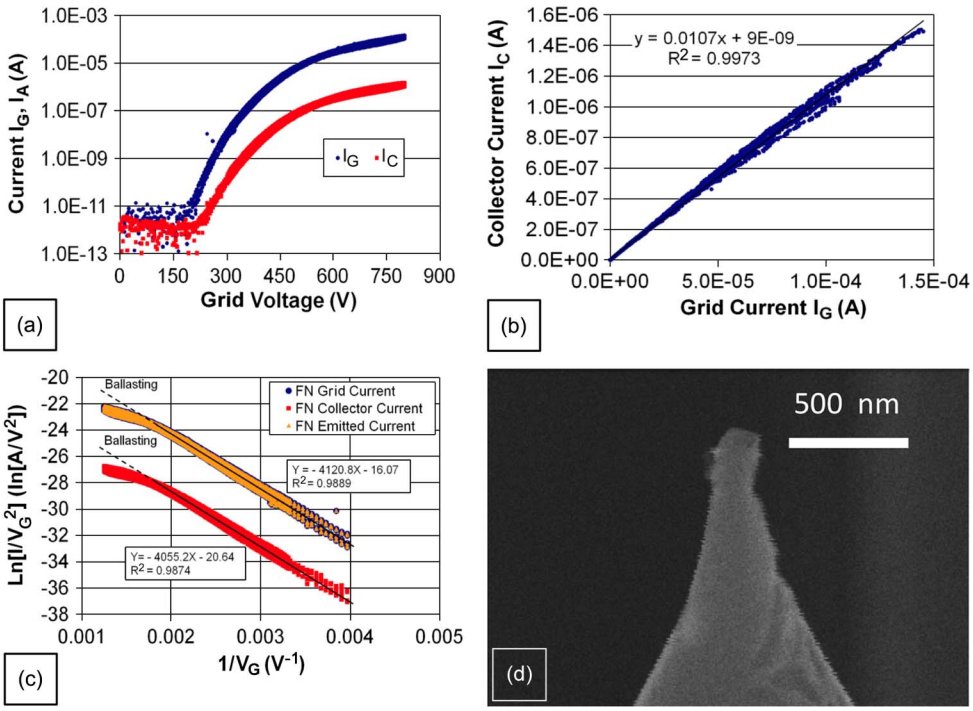


Fig. 6. Characterization of a one-million array of FEs individually controlled by ungated FETs made of lowly doped silicon: (a) I–V characteristics; (b) collector current versus grid current; (c) FN plot of the grid current and collector current; and (d) SEM of a typical FE.

radius from SEMs is about 87 nm. As expected, the typical FEA tip radius from SEMs is larger than the tip radius from the FN plot because at low-current emission, only the sharper tips are emitting. We should note that the FN slope was extracted at low extraction grid voltages in which emission current will be dominated by tips with radii much smaller than the average tip radius. For the doping level of the device, the saturation current per emitter from simulations is about 10 nA, as shown in Fig. 4. Therefore, roughly about 14 500 emitters (1.45% of the FEA) were active, while the FEA emitted 145 μA during the test.

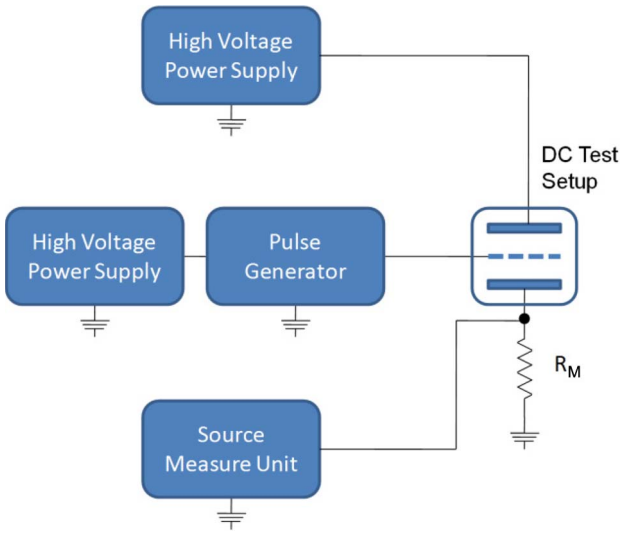


Fig. 7. Block diagram of the pulsed dc setup.

We can obtain an estimate of the tip radii variation based on the tip radius from the FN plot, the tip radius from the SEMs, and the estimate of the fraction of the FEA that was active if we assume a Gaussian tip radii distribution. We expect the typical tip radius from SEMs to be close to the average tip radius of the distribution because in a symmetrical statistical distribution, the mode of the distribution is equal to its mean [18]; we also expect the tip radius from the FN plot to be representative of the array of FEs that was active. A Gaussian distribution of a variable x can be normalized (i.e., mean equal to 0 and standard deviation equal to 1) if we use the transformation $Z = (x - \bar{x})/\sigma$, where σ and $\bar{x}$ are the standard deviation and the mean of x, respectively. Therefore, we estimated the variation in the tip radius Δ_r as

$$\Delta_r = \frac{r_{\mathrm{FN}} - r_{\mathrm{SEM}}}{Z};\ \%FEA_{\mathrm{ON}} = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{Z} \exp\left(-\frac{\theta^2}{2}\right) d\theta \tag{3}$$

where Δ_r is the estimated tip radii variation, r_{FN} is the tip radius from the FN plot, r_{SEM} is the typical tip radius from SEMs, $\%FEA_{\mathrm{ON}}$ is the percentage of the FEA that was active, and Z is the value of the normalized variable that corresponds to a cumulative Gaussian distribution equal to $\%FEA_{\mathrm{ON}}$. Using (3), we obtain $\Delta_r = 6.6$ nm, i.e., $r_{\mathrm{FN}} = r_{\mathrm{SEM}} - 2.19\Delta_r$. Therefore, the tip radii variation is about 7.5% the average tip radius.

B. Individually Ballasted FEAs, Pulsed I–V Characteristics

While conducting the dc experiments, we observed that the heat dissipated by the grid due to current interception limited the maximum emission current that could be sustained by the polymer gasket. We observed that at current levels above 1 mA, the heat dissipated by the grid reflowed the polymer gasket, which resulted in a lower voltage required to achieve the same emission current in subsequent tests. Eventually, the gasket shorted for devices that continuously emitted milliampere-level

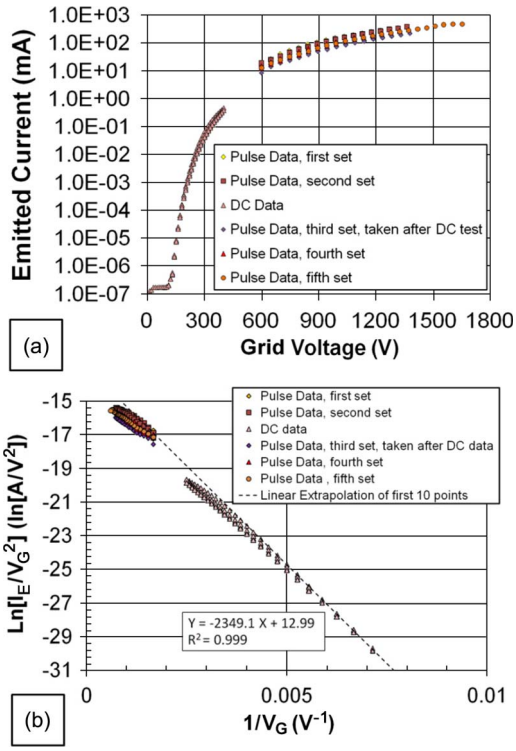


Fig. 8. Characterization of a one-million array of FEs individually controlled by ungated FETs made of silicon with a resistivity of 34.7 $\Omega \cdot$ cm: (a) I–V characteristics and (b) FN plot of the emission current.

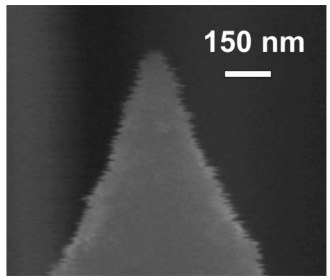


Fig. 9. SEM of a typical FE part of the individually ballasted FEA made of silicon with of 34.7 $\Omega \cdot$ cm resistivity. The tip radius is about 42 nm.

currents. As an estimate, 10 mA of emission current at a grid bias of 1000 V dissipated 10 W. Since most of the current is intercepted by the grid, most of the 10 W would heat up the grid (about 2.5 W/cm^2, comparable to the power density of a wafer helium-cooled reactive ion etcher). This level of heat dissipation should reflow the gasket. To avoid sustained heat dissipation while characterizing the FEAs, we implemented a pulsed setup. The setup also enabled us to obtain substantially larger emission currents, as well as to demonstrate complete current saturation at high voltage from an individually ballasted FEA made of silicon with a doping concentration of 2.4×10^{13} cm^{-3}.

Experimental Setup: A block diagram of the pulsed test rig is shown in Fig. 7. It is based on the dc test setup shown in Fig. 3, which is composed of the individually ballasted FEA, an unaligned perforated grid separated by a polymer gasket, and an external collector. In the pulsed test rig, the FEA is connected to the ground through a resistor R_M that is used to determine

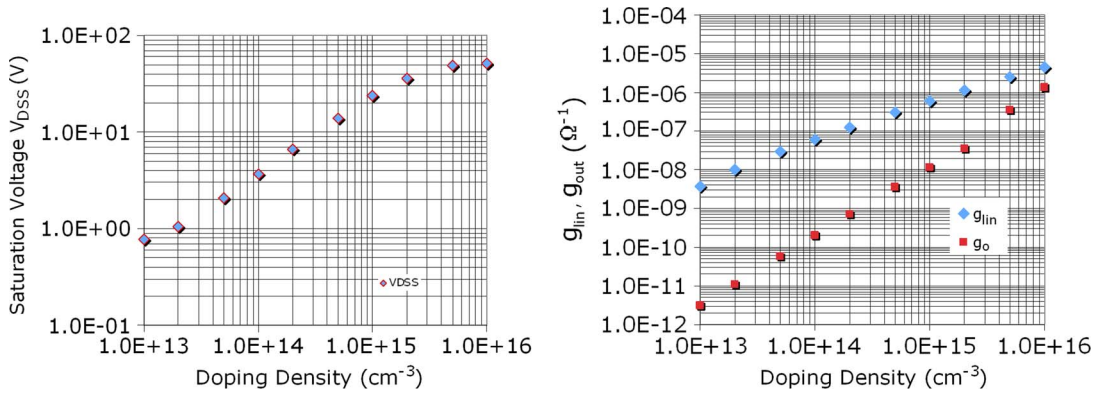


Fig. 10. Simulation estimates of the (left) drain–source saturation voltage $V_{\rm DSS}$ and (right) linear conductance $g_{\rm lin}$ and output conductance $g_{\rm out}$ versus doping concentration for a $1 \times 1 \times 100$ μm ungated Si FET.

the current emitted by the FEA. The grid voltage is supplied by a Glassman EQ1R1200 power supply that is controlled by a DEI PVX-4140 pulse generator. The collector electrode voltage is supplied by a Glassman LH3R1.721 power supply. Pulses of 2 μs with a period of 10 s were used to energize the grid. We verified that the pulse duration is long enough to produce a steady-state response from the FEAs, while the square wave period is long enough to substantially decrease the impact of the grid heat dissipation. We also verified the linearity between the collector current and the emitted current.

Medium-Doped Substrates, High Current: Fig. 8(a) is a plot of the pulsed I–V characteristics of a one-million array of FEs individually ballasted by ungated FETs that was fabricated on a silicon substrate with a resistivity of 34.7 $\Omega \cdot$ cm (doping concentration of 1.25×10^{14} cm^{-3}). The maximum emitted current per tip is 0.48 μA assuming uniform operation of the FEA. This is consistent with the maximum current $I_{\rm MAX} =$ 0.4 μA obtained at a bias of 100 V from simulations of the FET (Fig. 4). The FN plot of the emitted current obtained from pulsed tests is shown in Fig. 8(b). The plot clearly shows that for high grid voltage, the emission current is electron supply limited, whereas for lower applied grid voltages, the emission current is barrier limited. In the electron supply limited regime, the emitted current of 0.48 A is consistent with the saturation current of the ungated FET if one allows for the finite output resistance of the ungated FET. From the section of the FN plot for which electron emission is barrier limited, we estimated a field factor equal to 2.26×10^5 cm^{-1} using 4.05 eV as the workfunction for Si; the field factor corresponds to a tip radius of 32.5 nm if one uses (2) with $k_F = 2.5 \times 10^6$ and $n = 0.69$. The radius estimate is consistent with the tip radius of 42 nm from SEMs, as shown in Fig. 9. We should note that the FN slope was extracted from data at low extraction grid voltages in which the emission current is dominated by tips with radii smaller than the average tip radius. Based on the results of the simulations we made of the FET/FE structure [16] (Fig. 10), we estimate at $I_{\rm DSS} \times V_{\rm DSS} = 2.5$ μW the power dissipated by each vertical ungated FET when each FE emits 0.48 μA.

Lowly Doped Substrates, High Current: Fig. 11(a) is a plot of the pulsed I–V characteristics for an array of one million FEs individually controlled by vertical ungated FETs that was fabricated on a substrate with a resistivity of 178 $\Omega \cdot$ cm

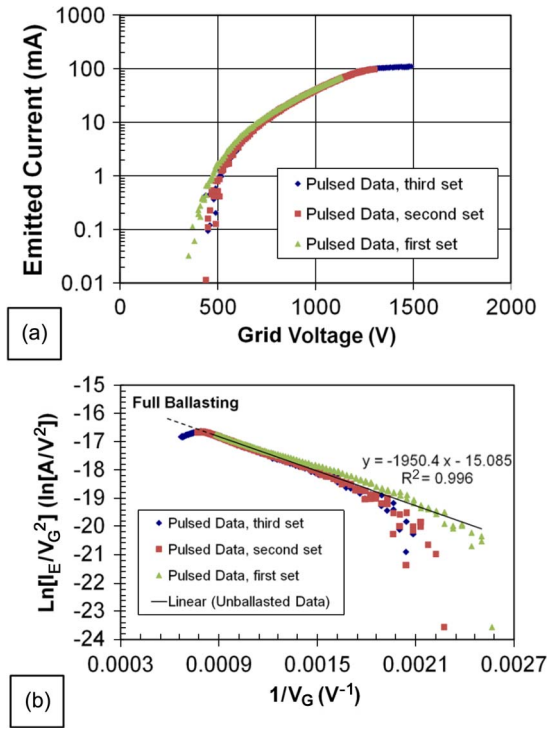


Fig. 11. Characterization of a one-million array of FEs individually controlled by ungated FETs made of silicon with a resistivity of 178 $\Omega \cdot$ cm: (a) I–V characteristics and (b) FN plot of the emission current.

(doping concentration of 2.4×10^{13} cm^{-3}). The emission current saturates at 0.109 A at grid voltages above 1200 V. The maximum emission current per tip is 109 nA, which is a factor of five larger than the 20 nA saturation current from simulations of the FET [16] (Fig. 4). Given the output conductance of the ungated FET, it is expected that the emission current will vary with the voltage drop across the ungated FET, particularly for the sharper tips. It is not clear at this time if this would account for the almost factor of five larger emission current per tip than the simulated ungated FET. Another potential source of additional current for the ungated FET is impact ionization at the drain region of the ungated FET due to the high voltage between the source and the drain. Also, impurity segregation into the silicon channel is expected to increase the channel doping, which should substantially increase the

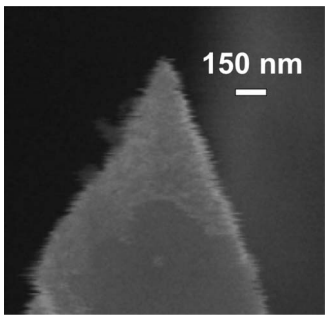


Fig. 12. SEM of a typical FE part of the individually ballasted FEA made of silicon with 178 $\Omega \cdot$ cm resistivity. The tip radius is about 33 nm.

carrier concentration in lowly doped substrates. The FN plot of the emitted current obtained from the pulsed tests is shown in Fig. 11(b). At low voltages, the slope of the FN plot is constant and negative, corresponding to the region dominated by electron transmission through the barrier. However, the slope becomes positive at high voltages (> 1200 V) corresponding to the region dominated by electron supply to the barrier, as previously shown by Hong and Akinwande [13] for FEAs ballasted by a MOSFET. From the region in which electron emission is controlled by transmission through the barrier, we extracted a field factor equal to 2.73×10^5 cm^{-1}, which corresponds to a tip radius if 24.8 nm if we use (2) with $k_F = 2.5 \times 10^6$ and $n = 0.69$. This is consistent with the tip radius of 33 nm from the SEMs as shown in Fig. 12. We should note that the FN slope was extracted from data at low extraction grid voltages in which the emission current is dominated by tips with radii smaller than the average tip radius. Based on the results of the simulations we made of the FET/FE structure [16] (Fig. 10), we estimate at $I_{\rm DSS} \times V_{\rm DSS} = 0.13$ μW the power dissipated by each vertical ungated FET when each FE emits 109 nA.

IV. Discussion

Very little has been reported in the literature on two-terminal current limiters. In order to obtain current limitation, resistors or transistors are often used, the latter with the added need to bias the third terminal. The earliest two-terminal current limiter reported in the literature was by Boll *et al.*, which used diffused contacts into germanium to obtain current-source-like behavior from an gated FET structure. They attributed the current limitation to the velocity saturation of carriers in Ge [19]. Baek *et al.* [20] reported work on ungated GaAs MESFET structure that has essentially the same structure as that of Boll *et al.*, with the exception that the substrate is now GaAs and the contacts were ion implanted. Again, Baek *et al.* explained their results using velocity saturation of carriers in GaAs. This work builds on the results reported by Boll and Baek, which used very closely spaced contacts in order to attain high fields and, hence, saturation velocity at relatively small voltages. This work also invokes velocity saturation of carriers. However, in this case, the contacts are not closely spaced but, rather, the contacts are spaced much further apart. Velocity saturation is attained by pinching off the channel at the drain end by the drain-to-source voltage. Pinchoff is easily attained for a Si column with narrow width, i.e., high-aspect-ratio column. Using a wider column leads to a higher drain voltage for the channel to pinchoff.

When the Si column ungated FET is integrated with the FE, we observe that the emitted current is limited by the ungated FET. This is consistent with prior work on the control of emission current from FE arrays by transistors [13] and the other preceding literature reports by Itoh *et al.* [21], Kanemaru *et al.* [22], and Nagao *et al.* [23]. Takemura *et al.* [12] reported a silicon current limiter based on trench etching of Si, oxide filling, and planarization. However, they did not attempt to control emission current from individual emitters. When the current limiter is used with a group of FEs, it provides current limitation at high current levels. This is consistent with the fact that the current limiter did not have a high aspect ratio and the columns cross-sectional area was relatively big (4×4 μm). This means that the current through the columns will only saturate at very high current levels. Using the work reported by Takemura *et al.*, Imura *et al.* reported remarkable reliability from the FEAs that were used in a demonstration of very-high-performance traveling wave tubes [24]. The silicon columns provided current limitation to an array of FE at very high current levels, thus enhancing reliability of the array. The current limiters enhance reliability at the array level but do not necessarily prevent burnout of the sharpest emitter tips within the array nor enhance uniformity. Also, the high currents are well above the operating regime of the tubes. Our device architecture is better because it provides individual current limitation to each tip using a high-aspect-ratio silicon column, resulting in uniform and reliable FE arrays.

We have operated FE arrays that are individually ballasted for continuous periods longer than 20 h. The device operated at the instrument current compliance limit of 10 mA with an applied gate to emitter voltage > 600 V. Since the 95% of the emitted current was intercepted by the gate, this implies than about 5.5 W was dissipated in the structure resulting in a temperature increase and partial melting or softening of the spacer, which led to the reduction in the spacing between the gate and the emitter and, consequently, an increase in the current until current compliance in the instrument was reached. This eventually resulted in a short between the gate and the emitter. However, each time, the spacer was replaced and the device went back to approximately the same operating conditions after adjusting for changes in spacer thickness. There was never any evidence of emitter tip burnout from Joule heating, suggesting that the Si column ungated FET was effective in limiting current through the FE. More systematic study of the effect of the Si column current limiter on the emitter tip lifetime needs to be conducted.

V. Conclusion

We have demonstrated high-current electron sources that achieve uniform emission using large and dense arrays of individually ballasted Si FEs. Each FE is fabricated on top of a vertical ungated FET. The ungated FET achieves current-source-like behavior due to the velocity saturation of electrons in silicon, the very high aspect ratio of the ungated FET, and the doping concentration. Evidence of full ballasting was provided. Emitted currents in excess of 0.48 A were demonstrated.

ACKNOWLEDGMENT

The authors would like to thank the staff of MIT's Microsystems Technology Laboratories (MTL) for their help in the fabrication of the structures.

REFERENCES

[1] J. D. Lee, I. H. Kim, C. W. Oh, J. W. Park, and B. G. Park, "MOSFET-controlled field emission display (MCFED)," in *Proc. 14th Int. Vacuum Microelectron. Conf.*, 2001, pp. 189–190.

[2] S. Kanemaru, T. Hirano, K. Honda, and J. Itoh, "Stable emission from a MOSFET-structured emitter tip in poor vacuum," *Appl. Surf. Sci.*, vol. 146, no. 1, pp. 198–202, May 1999.

[3] S. C. Lim, R. E. Stallcup, II, I. A. Akwani, and J. M. Perez, "Effects of O_2, H_2, and N_2 gases on the field emission properties of diamond coated microtips," *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1179–1181, Aug. 1999.

[4] K. Teo, E. Minoux, L. Hudanski, F. Peauger, J.-P. Schnell, L. Gangloff, P. Legagneux, D. Dieumgard, G. Amaratunga, and W. Milne, "Microwave devices: Carbon nanotubes as cold cathodes," *Nature*, vol. 437, no. 7061, p. 968, Oct. 2005.

[5] L.-Y. Chen, L. F. Velásquez-García, X. Wang, K. Teo, and A. I. Akinwande, "A micro ionizer for portable mass spectrometers using double-gated isolated vertically aligned carbon nanofiber arrays," in *IEDM Tech. Dig.*, Washington, DC, Dec. 2007, pp. 843–846.

[6] W. Milne, K. Teo, M. Mann, I. Bu, G. Amaratunga, N. De Jonge, M. Allioux, J. Oostveen, P. Legagneux, E. Minoux, L. Gangloff, L. Hudanski, J.-P. Schnell, D. Dieumegard, F. Peauger, T. Wells, and M. El-Gomati, "Carbon nanotubes as electron sources," *Phys. Stat. Sol. (A)*, vol. 203, no. 6, pp. 1058–1063, May 2006.

[7] R. Gomer, *Field Emission and Field Ionization*. New York: Amer. Inst. Phys., 1961.

[8] M. Ding, G. Sha, and A. I. Akinwande, "Silicon field emission arrays with atomically sharp tips: Turn-on voltage and the effect of tip radius distribution," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2333–2342, Dec. 2002.

[9] D. G. Pflug, M. Schattenburg, H. I. Smith, and A. I. Akinwande, "Field emitter arrays for low voltage applications with sub 100 nm apertures and 200 nm period," in *IEDM Tech. Dig.*, Dec. 2001, pp. 179–182.

[10] L. Nilsson, O. Groening, O. Kuettel, P. Groening, and L. Schlapbach, "Microscopic characterization of electron field emission," *J. Vac. Sci. Technol. B*, vol. 20, no. 1, pp. 326–337, Jan. 2002.

[11] J.-M. Bonard, K. A. Dean, B. F. Coll, and C. Klinke, "Field emission of individual carbon nanotubes in the scanning electron microscope," *Phys. Rev. Lett.*, vol. 89, no. 19, pp. 197602-1–197602-4, Nov. 2002.

[12] H. Takemura, Y. Tomihari, N. Furutake, F. Matsuno, M. Yoshiki, N. Takada, A. Okamoto, and S. Miyano, "A novel vertical current limiter fabricated with a deep-trench-forming technology for highly reliable field emitter arrays," in *IEDM Tech. Dig.*, Dec. 1997, pp. 709–712.

[13] C.-Y. Hong and A. I. Akinwande, "Temporal and spatial current stability of smart field emission arrays," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2323–2328, Oct. 2005.

[14] P. Vaudiane and R. Meyer, "Microtips fluorescent display," in *IEDM Tech. Dig.*, Dec. 1991, pp. 197–200.

[15] L. F. Velásquez-García, B. Adeoti, Y. Niu, and A. I. Akinwande, "Uniform high current field emission of electrons from Si and CNF FEAs individually controlled by Si pillar ungated FETs," in *IEDM Tech. Dig.*, Washington, DC, Dec. 2007, pp. 599–602.

[16] L. F. Velásquez-García, S. A. Guerrera, Y. Niu, and A. I. Akinwande, "Uniform high-current cathodes using massive arrays of Si field emitters individually controlled by vertical Si ungated FETs—Part 1: Device design and simulation," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1775–1782, Jun. 2011.

[17] L. Dvorson, G. Sha, I. Kymissis, C.-Y. Hong, and A. I. Akinwande, "Electrical and optical characterization of field emitter tips with integrated vertically stacked focus," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2548–2558, Dec. 2003.

[18] S. Ross, *A First Course in Probability*, 4th ed. Englewood Cliffs, NJ: Prentice-Hall, 1994, p. 215.

[19] H. J. Boll, J. E. Iwersen, and E. W. Perry, "High speed current limiters," *IEEE Trans. Electron Devices*, vol. ED-13, no. 12, pp. 904–907, Dec. 1966.

[20] J. Baek, M. S. Shur, K. W. Lee, and T. Vu, "Current–voltage characteristics of ungated GaAs FETs," *IEEE Trans. Electron Devices*, vol. ED-32, no. 11, pp. 2426–2430, Nov. 1985.

[21] J. Itoh, T. Hirano, and S. Kanemaru, "Ultrastable emission from a metal–oxide–semiconductor field-effect transistor-structured Si emitter tip," *Appl. Phys. Lett.*, vol. 69, no. 11, pp. 1577–1578, Sep. 1996.

[22] S. Kanemaru, T. Hirano, H. Tanoue, and J. Itoh, "Control of emission currents from silicon field emitter arrays using a built-in MOSFET," *Appl. Surf. Sci.*, vol. 111, pp. 218–223, Feb. 1997.

[23] M. Nagao, Y. Tamura, T. Matsukawa, S. Kanemaru, J. Itoh, and K. Tokunaga, "Fabrication of Si field emitter arrays integrated with metal–oxide–semiconductor field-effect transistor driving circuits," *J. Vac. Sci. Technol. B*, vol. 20, no. 6, pp. 2309–2313, Nov. 2002.

[24] H. Imuira, S. Tsuida, M. Takaha, A. Okamoto, H. Makishima, and S. Miyano, "Electron gun design for traveling wave tubes (TWTs) using a field emitter array (FEA) cathode," in *IEDM Tech. Dig.*, Dec. 1997, pp. 721–724.

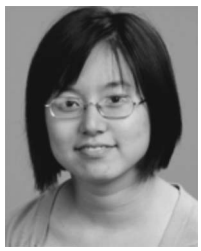
Luis Fernando Velásquez-García (M'09–SM'10) received the Mechanical Engineer and Civil Engineer degrees (*magna cum laude* and valedictorian of the School of Engineering in both degrees) from the Universidad de Los Andes, Bogotá, Colombia, in 1998 and 1999, respectively, and the M.S. and Ph.D. degrees from the Department of Aeronautics and Astronautics, Massachusetts Institute of Technology (MIT), Cambridge, in 2001 and 2004, respectively.

In 2004, after completing his studies, he became a Postdoctoral Associate in the Microsystems Technology Laboratories (MTL), MIT, where he was appointed as a Research Scientist in 2005. Since 2009, he has been a Principal Scientist and Core Member with MTL. He is an expert in microfabrication and nanofabrication technologies, and his research focuses on the application of microtechnology and nanotechnology to multiplexed scaled-down systems to attain better performance. He has conducted research in microtechnologies and nanotechnologies applied to electrospray, carbon-nanotube-based devices, 3-D packaging, mass spectrometry, nanosatellite propulsion and scientific payload, and chemical reactors. He is the author of more than 17 journal publications and 30 conference proceedings entries. He is the holder of six patents on MEMS technologies.

Dr. Velásquez-García is a Full Member of Sigma Xi and a Senior Member of the American Institute of Aeronautics and Astronautics.

Stephen A. Guerrera (S'07) received the B.S. degree (*summa cum laude*) in electrical and computer engineering from Northeastern University, Boston, MA, in 2008. He is currently working toward the M.S. degree in the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge.

His current research interests include vacuum microelectronics, particularly field emission and field ionization devices, and microfabrication/nanofabrication technologies.



Ying Niu (M'09) received the B.S. and M.Eng. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 2008 and 2009, respectively.

She is currently a Systems Engineer II with the Integrated Defense Systems division of Raytheon Corporation, Fort Wayne, IN. He is also a member of the Raytheon Leadership Development Program, Class of 2012.

Akintunde Ibitayo (Tayo) Akinwande (S'81–M'86–SM'04–F'08) received the B.Sc. degree in electrical and electronics engineering from the University of Ife, Ife, Nigeria, in 1978 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1981 and 1986, respectively.

In 1986, he joined Honeywell International, Inc., Morristown, NJ, where he initially conducted research on GaAs complementary FET technology for very-high-speed and low-power signal processing. He later joined the Si Microstructures Group, where he conducted research on pressure sensors, accelerometers, and thin-film field emission and display devices. In January 1995, he joined the Microsystems Technology Laboratories, Massachusetts Institute of Technology (MIT), Cambridge, where his research focuses on microfabrication and electronic devices, with particular emphasis on smart sensors and actuators, intelligent displays, large-area electronics (macroelectronics), field emission and field ionization devices, mass spectrometry, and electric propulsion. He was a Visiting Professor in the Department of Engineering and an Overseas Fellow at Churchill College, Cambridge University, Cambridge, U.K., in 2002 and 2003. He is currently a Professor in the Department of Electrical Engineering and Computer Science, MIT. Since September 2009, he has been a Program Manager of the Microsystems Technology Office, Defense Advanced Research Projects Agency. He is the author of more than 100 journal publications. He is the holder of numerous patents in the areas of MEMS, electronics on flexible substrates, and display technologies.

Prof. Akinwande was the recipient of a 1996 National Science Foundation CAREER Award. He is currently a member of the IEEE Nanotechnology Council. He has served on a number of Technical Program Committees for various conferences, including the Device Research Conference, the IEEE International Electron Devices Meeting, the IEEE International Solid-State Circuits Conference, the International Display Research Conference, and the International Vacuum Microelectronics Conference.