Scaling of High-Aspect-Ratio Current Limiters for the Individual Ballasting of Large Arrays of Field Emitters

Stephen A. Guerrera, *Student Member, IEEE*, Luis Fernando Velásquez-García, *Senior Member, IEEE*, and Akintunde Ibitayo Akinwande, *Fellow, IEEE*

***Abstract*—We report the fabrication and characterization of high-aspect-ratio silicon pillar current limiters [vertical ungated field-effect transistors (FETs)] for ballasting individual field emitters within field-emitter arrays (FEAs). Dense (1-μm pitch) FEAs that are individually ballasted by 100-nm-diameter and 10-μm-tall current limiters were fabricated, resulting in an emitter tip radius under 10 nm. When characterized without field emitters, the vertical current limiters (ungated FETs) show current-source-like behavior, with saturation currents up to 15 pA/FET. When the current limiters are incorporated into large arrays of field emitters, the current–voltage characteristics of the FEA show evidence of current limitation at high extraction gate voltages. Emission current densities of over 200 μA/cm^2 were obtained from 1.36 million emitter arrays with 5-μm pitch.**

***Index Terms*—Ballasting, cathodes, electron supply control, Si field-emission arrays, vertical ungated Si field-effect transistors (FETs).**

I. Introduction

FIELD-EMITTER ARRAYs (FEAs) are excellent cold cathodes; however, they have not found widespread adoption in demanding device applications because of several major challenges, the most significant of which is spatial and temporal nonuniformities. Spatial nonuniformities typically result from variations in emitter tip radius, and since all FEAs have nonzero tip radius distribution [1], subutilization of the array elements often results. For example, sharper emitters burn out from Joule heating before duller emitters turn on reducing the overall current density and the total emission current attainable from FEAs.

To address these nonuniformities, researchers have incorporated current-limiting (ballasting) elements such as large resistors [2] and MOSFETs [3], [4] into FEAs; however, neither of these solutions simultaneously provide high emitter density, high current density, and high current. A robust solution of the uniformity problem requires individual control of each field emitter by a suitable ballasting element. Several researchers have demonstrated a Si tip-on-Si pillar structure [5]–[8]; however, only Velásquez-García *et al.* used the Si pillar as a current limiter to improve uniformity [8]. The work reported in [5] and [6] used the Si post to decrease the capacitance between the gate and the substrate to allow higher frequency operation, while Takemura *et al.* [7] used the pillar to improve reliability.

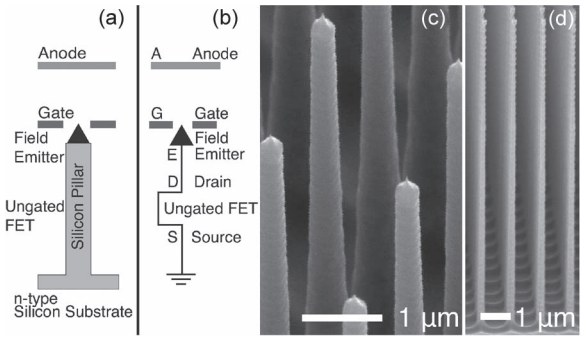

Fig. 1. (a) Schematic diagram of a single field emitter ballasted by an ungated FET. (b) Circuit diagram of the FET–FEA structure. (c) SEM image of the completed FET–FEA structure. (d) Cross-sectional SEM image of an ungated FET current limiter without a field emitter with oxide removed to show the pillar.

In Fig. 1, a schematic drawing [Fig. 1(a)] and equivalent circuit diagram [Fig. 1(b)] of the FEA and current-limiting device are shown. The vertical current limiter (ungated FET) has a current-source-like I–V characteristic when biased at voltages larger than its saturation voltage [9], [10]. To limit the emission current, the vertical ungated FET uses pinchoff and velocity saturation of majority carriers at high fields in a high-aspect-ratio silicon channel.

When vertical current limiters are connected in series with individual field emitters, they limit the current from each field emitter in the array, allowing for uniform emission without thermal runaway or burnout, provided that their saturation current is below the burnout limit [8], [11]. This current limitation is consistent with the operation of the device in the electron-supply-controlled regime instead of the electron-transmission-controlled regime as observed by Ding *et al.* for Si FEAs [4], [12] allowing for reliable operation of FEAs at high currents.

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The combined vertical ungated FET–FEAs reported by Velásquez-García *et al.* in [13] had Si pillars with a diameter of 1 μm, a height of 100 μm, and 10-μm pitch, resulting in a density of 10^6 tips/cm^2. The FEAs are capable of high and uniform current emission (0.5 A and 0.5 A/cm^2). With an integrated self-aligned gate, the devices should have a gate aperture roughly equal to the Si pillar diameter [14], resulting in turn-on voltages of approximately 25 V and operating voltages of 75–100 V [1].

Reducing all of the dimensions of the current limiter–FEA structure provides several benefits. By shrinking the pitch of the emitters, the tip density is increased. Because the pillar cross-sectional area is smaller, the saturation current for a given doping density is lower; however, by increasing the doping in the pillar, the current density increases, allowing the same current per emitter to be obtained from narrower pillars. In addition, the gate aperture scales with the pillar diameter. Thus, by decreasing the pillar diameter—and, by implication, the gate aperture—the field factor β (cm^{-1}), which relates the gate voltage to the electrostatic field at the tip surface, increases, resulting in lower turn-on and operating voltages. In practice, Pflug *et al.* demonstrated gate apertures as small as 70 nm, resulting in a turn-on voltage of 8.5 V [15].

A consequence of using vertical ungated FETs to limit the current from FEAs is the larger energy spread of the emitted electrons when compared to unballasted FEAs. In an unballasted FEA, each emitter in the array has the same gate–emitter voltage bias. However, when a vertical ungated FET current limiter controls the current through each emitter, the gate voltage V_G is divided between the gate–emitter voltage $V_{\rm GE}$ and the drain–source voltage $V_{\rm DS}$ of the vertical current limiter, i.e., $V_G = V_{\rm GE} + V_{\rm DS}$. Because each emitter is biased at a different gate–emitter voltage, electrons from each emitter are accelerated by different voltages, resulting in a wider energy distribution. The energy spread of the FEA current can be reduced by shrinking the gate aperture, and thus increasing β, while keeping its uniformity constant. Using a FEM simulation platform, we estimated that, by increasing β by a factor of five while keeping the same tip radius statistics, the energy spread across the FEA decreased from 5 to 2 eV.

To obtain FEAs with higher current densities, lower operating voltages, and reduced energy spread while retaining current uniformity, we expanded on the work of Velásquez-García *et al.* by decreasing the diameter and pitch of their tip-on-Si pillar structure by an order of magnitude while keeping the same aspect ratio. We have fabricated scaled current limiter/FEAs with 1-μm pitch, 100-nm diameter, and 10-μm pillar height [Fig. 1(c)]. However, we were unable to test them using a suspended extraction gate, as electric field screening from nearby pillars rendered it impossible to obtain a sufficiently high field factor. Two-dimensional electrostatic simulations indicate that, at 1-μm pitch, an extraction gate voltage in excess of 10 kV is required for field emission without a proximal gate. This voltage exceeds the dielectric strength of the polymer spacer used in our field-emission testing apparatus.

Thus, the focus of this paper is on the following: 1) the fabrication and characterization of vertical ungated FET current limiters that are 100 nm in diameter and 8 μm tall and have 1-μm pitch, resulting in a density of 10^8 cm^{-2}, and 2) the fabrication and characterization of FEAs individually ballasted by vertical ungated FET current limiters that are 10 μm tall and have a pitch of 5 μm.

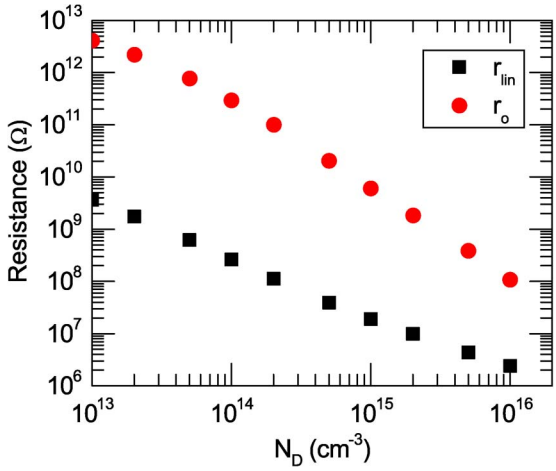

Fig. 2. Simulated linear resistance ($r_{\rm lin}$) and output resistance (r_O) versus donor concentration, for a fixed channel length of 10 μm.

II. Simulation of Vertical Current Limiters

To estimate the performance of the vertical ungated FET current limiters and serve as a guide to their fabrication, extensive process and device simulations were performed using the SILVACO toolset (Silvaco International, Santa Clara, CA). For these simulations, the Si pillar cross-sectional area was fixed at 100 nm $\times$ 100 nm. The area surrounding the pillar was filled with SiO_2, and both the top drain contact and substrate source contact were assumed to be perfect ohmic contacts. No interface states or fixed charge at the $Si-SiO_2$ interface was included in these simulations.

Once the structure was obtained, ATLAS was used to simulate the current–voltage characteristics of a single vertical ungated FET current limiter. These simulations solved Poisson's equation self-consistently with the carrier flow and continuity equations. To explore the functional dependences on channel length and doping, the doping density N_D was varied between 10^{13} and 10^{16} cm^{-3}, and the channel length L was varied between 1 and 10 μm. For the simulations where N_D was varied, the channel length was fixed at 10 μm, and for the simulations where L was varied, N_D was fixed at 5×10^{14} cm^{-3}.

The linear resistance ($r_{\rm lin}$), the output resistance, (r_o), and the drain saturation current per pillar ($I_{\rm DSS}$) were extracted from the simulations. The dependences of r_o and $r_{\rm lin}$ (Fig. 2) and $I_{\rm DSS}$ (Fig. 3) on the doping density are plotted in Figs. 2 and 3. In Figs. 4 and 5, the dependences of r_o and $r_{\rm lin}$ (Fig. 4) and $I_{\rm DSS}$ (Fig. 5) on the channel length are shown. An aspect ratio greater than 50 : 1 is required to obtain a sufficiently large dynamic resistance while simultaneously providing the large current per tip required for high-performance FEAs. We followed the sensitivity analysis approach originally proposed by Hong and Akinwande [4] and adopted by Velásquez-García *et al.* [8] to determine the dynamic resistance ($r_o = 10^{11}$ Ω) required for uniform emission current.

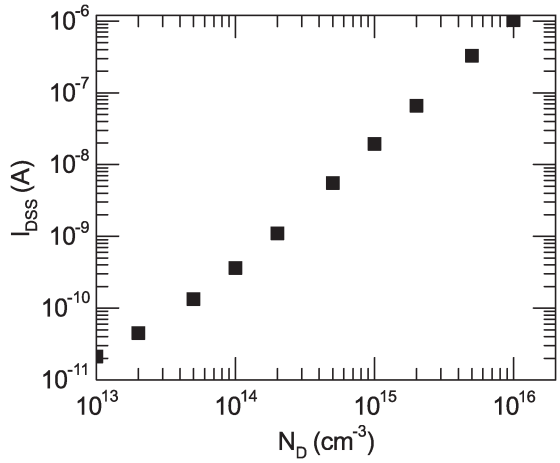

Fig. 3. Simulated drain saturation current $(I_{\rm DSS})$ versus donor concentration for a fixed channel length of 10 μm.

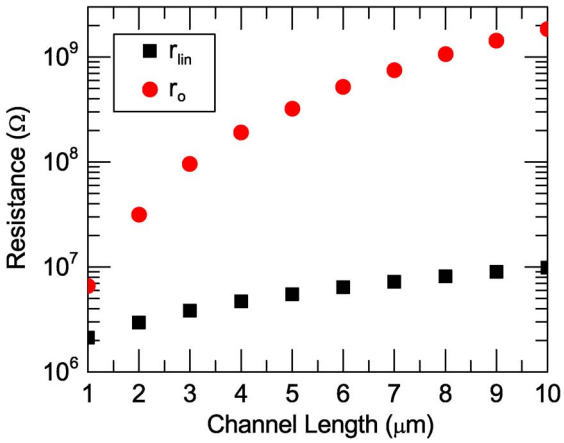

Fig. 4. Simulated $r_{\rm lin}$ and r_O versus channel length, for a fixed N_D of 5×10^{14} cm^{-3}.

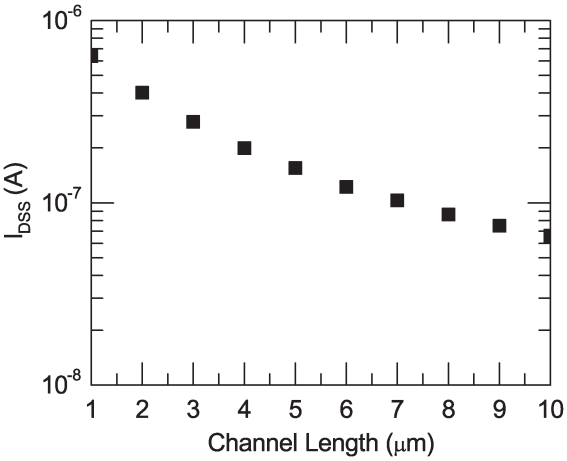

Fig. 5. Simulated $I_{\rm DSS}$ versus channel length for a fixed N_D of 5×10^{14} cm^{-3}.

Increasing the aspect ratio much beyond 100 : 1, however, gives diminishing returns, with all three parameters approaching asymptotic values. In addition, current limiters with aspect ratios larger than 100 : 1 further complicate fabrication. Based on these simulations, wafers with a doping density of 2×10^{14} cm^{-3} and a target pillar height of 10 μm (corresponding to a pillar aspect ratio of 100 : 1) were chosen to theoretically obtain devices with a saturation current of 1 nA/pillar and an output resistance greater than 10^{11} Ω.

III. Fabrication of Vertical Current Limiters

Large arrays (3.6×10^7 devices) of vertical current limiters without field emitters were fabricated using 6-in n-Si wafers. First, a 0.3-μm thermal SiO_2 hardmask is grown. Using an i-line wafer stepper, photolithography is performed to create photoresist dots approximately 500 nm in diameter with 1-μm pitch. These dots are used to pattern the oxide film in a CF_4/CHF_3/Ar reactive ion etcher (RIE). The vertical current limiters are next etched using a Bosch process deep RIE (DRIE). Following this step, the photoresist and any polymers remaining from the passivation step of the DRIE are etched (ashed), and the oxide is removed in 50% HF. An RCA clean is performed, and a thermal oxide film is grown both to passivate and smooth the silicon pillar surface and to further reduce the dimensions of the pillar. Fig. 1(d) shows a cross-sectional SEM image of the vertical current limiters after this oxidation-thinning step with the oxide removed, demonstrating a pillar diameter of 93 nm at the thinnest point.

To make top contact to the pillars, the remaining gaps between the pillars are filled in with dielectric. A 600-nm-thick LPCVD low-temperature oxide is deposited, and then, 0.5 μm of undoped poly-Si is deposited using LPCVD to fill in the remaining gaps. Then, 75% of the poly-Si on the surface is removed through oxidation and subsequent etching in HF, and contact windows to the vertical current limiters are opened using RIE after the remaining poly-Si is oxidized.

Finally, a shallow ion implantation of arsenic was performed, annealed, and activated at 950 °C in an N_2 ambient. Then, a metal stack consisting of a 100-nm TiN diffusion barrier and 1-μm Al was sputtered to form ohmic contacts to Si. The metallization was patterned using photolithography and Cl_2 plasma, and the metallization was annealed at 400 °C under forming gas.

IV. I–V Characterization and Analysis of Scaled Vertical Current Limiters

I–V characterization took place in a probe station using an Agilent 4156C semiconductor parameter analyzer. During the measurement, the substrate (and the source end of the channel) was held at 0 V, and a positive voltage $V_{\rm DS}$ was applied to the drain contact. Table I is a summary of experimental I–V measurements performed. In general, the devices demonstrate current saturation, with a saturation current $(I_{\rm DSS})$ of approximately 15 pA/pillar and an output conductance $(g_{\rm lin})$ less than 1.8×10^{-13} S/pillar. The current saturates at a drain-to-source saturation voltage $(V_{\rm DSS})$ under 0.2 V. A linear conductance $(g_{\rm lin})$ of up to 2.6×10^{-10} S/pillar was measured. To ensure that the resistance was not a direct result of contact resistance, transfer length measurements (TLMs) were performed. From the TLM structures, a specific contact resistance of 3.2×10^{-3} Ω/cm^2 was obtained, resulting in an estimated contact resistance of 3.80×10^7 Ω to the pillar, which is several orders

TABLE I
MEASURED CURRENT–VOLTAGE CHARACTERIZATION DATA

Size of Array	I_{DSS}/pillar [pA]	V_{DSS} [V]	g_{lin}/pillar [pS]	g_{out}/pillar [pS]
1	8.5	0.06	150	0.33
4	0.50	0.20	6.7	0.18
5	1.3	0.20	12	0.061
8	2.2	0.80	28	0.096
62.5k	2.6	0.01	23	-[a]
125k	1.8	0.08	22	-
250k	1.9	0.06	33	-
500k	2.1	0.06	38	0.0060
1M	15	0.15	250	0.090
2M	10	0.08	42	0.022
4M	4.7	0.05	99	0.0065

a. Indicates negative resistance in the saturation regime

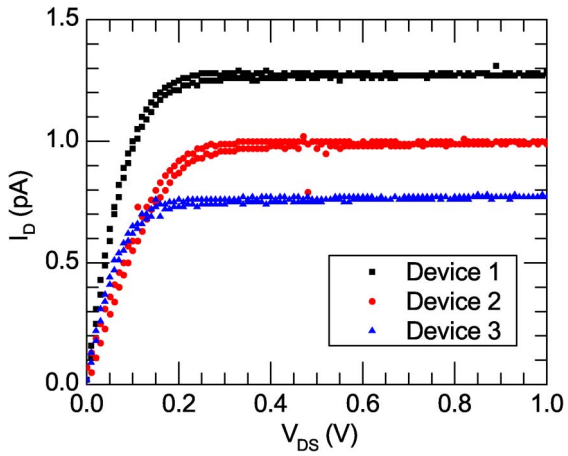

Fig. 6. I–V characteristics of three different single vertical current limiters on a single die exhibiting process and/or doping variation.

of magnitude less than the linear resistance. The aforementioned extraction of contact resistance likely underestimates the contact resistance to the pillars, as the contact openings in the TLM test structures were 300 μm $\times$ 10 μm, whereas the pillar cross section is 100 nm $\times$ 100 nm.

Fig. 6 shows the I–V characteristics for several single current limiters in a single array, and Fig. 7 shows an I–V characteristic for an array of 4M current limiters. In both cases, the I–V characteristic provides evidence for the current-limiting capabilities of the scaled current limiter structure. Our simulation results predicted that the saturation current, output conductance, and linear conductance should have been a factor of 30 larger than what was extracted from I–V characterization of the fabricated devices. We do not have a specific explanation for the discrepancy between the device simulation and our measurements. We speculate that this discrepancy could be primarily caused by the low doping in the channel. With a doping density of 2×10^{14} cm^{-3}, assuming a Poisson distribution of dopant atoms, there are approximately 35 donor atoms in the entire 10-μm-long channel. Because of the small number of dopant atoms, we expect random dopant fluctuations (RDFs) and interface traps at the Si/SiO_2 interface to have an impact on the vertical silicon ungated FET current limiters. While RDF and interface traps typically manifest themselves as threshold voltage shifts in MOS devices [16]–[18], in the

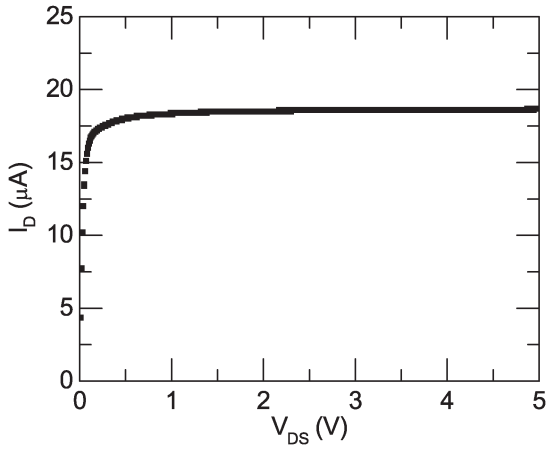

Fig. 7. I–V characteristic of an array of 4M vertical current limiters.

vertical current limiter, RDF and interface traps directly affect the channel conductivity and, in large part, explain the variation of saturation currents and linear conductivities measured in the actual devices. For a particular doping density and pillar diameter, simulations suggest that it is possible to pinch off the channel even when there is no applied voltage given a sufficiently high interface trap density. This results in much reduced drain currents. These deleterious effects could be substantially curtailed if the doping density is increased to at least 1×10^{15} cm^{-3}. Another source of conductivity variation is pillar diameter variation, arising from nonuniformities in fabrication, particularly in the photolithography and etching steps.

V. THERMAL RUNAWAY AND FAILURE ANALYSIS OF VERTICAL CURRENT LIMITERS

To explore the ultimate performance and failure mode of the current limiters, an analysis of the thermal breakdown of the silicon pillars was performed. Experiments were conducted to verify the maximum possible current sourced before failure of the vertical current limiters. Several single vertical current limiters were characterized using an Agilent 4156C semiconductor parameter analyzer under conditions where current was varied and voltage was measured until thermal runaway and device failure occurred. Fig. 8 shows a representative voltage–current characteristic, which exemplifies the failure that occurred. I–V characteristics of the device were taken before and after stressing. Before stressing, the device had a saturation current of 8 pA. At a bias current of 11 pA, impact ionization in the high-field region of the channel was observed, resulting in a large change in current with small increase in voltage. At a current level of 200 nA, the device failed, and the measured voltage reached the testing compliance limit, indicating that an open circuit has formed. The inset of Fig. 8 shows an optical micrograph of the metal contact pad after stressing, showing physical damage resulting from the destructive testing: a large crater in the metallization centered on the location of the single pillar contact.

Following the analysis of the thermal limits of field emitters presented by Utsumi in [11], the maximum current density at

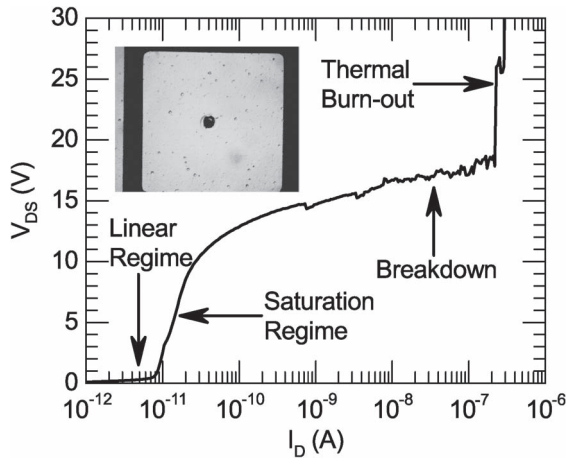

Fig. 8. Voltage–current stressing sweep resulting in thermal runaway and breakdown. Breakdown occurred at 2×10^{-7} A. (Inset) After stressing, there is visible damage to the metallization.

burnout due to Joule heating approximated by

$$J_{\max} = \frac{\sqrt{2T_m\widetilde{\sigma}k}}{h}(\mathrm{A/cm^2}) \quad (1)$$

where h is the height of the structure, T_m is the melting temperature of silicon, $\widetilde{\sigma}$ is the average value of electrical conductivity, taken between room temperature and T_m, and k is the thermal conductivity of silicon. Using the thermal conductivity and electrical conductivity values for n-type silicon with a donor concentration of 2×10^{14} cm^{-3}, a value of 100 nA for $I_{\max}(I_{\max} = J_{\max} \times$ cross-sectional area) is obtained for a 100-nm-diameter column, agreeing with the experimental value of 200 nA to within a factor of two.

VI. Fabrication of FEAs Individually Ballasted by Vertical Current Limiters

The combined ungated FET current limiter–FEA structure was fabricated with 5-μm pitch and hexagonal packing. The fabrication begins identically to the vertical current limiter structure described in Section III. After the patterning of the oxide in the RIE tool, the initial formation of the emitter cones is performed using RIE with SF_6/O_2 chemistry. The partial pressure of oxygen changes the lateral etch rate while barely changing vertical etch rate, allowing for control over the etch. The undercutting step needed to be precisely controlled to obtain a sharp tip after the oxidation to reduce the pillar diameter. After the tip formation, the pillar is etched using the same DRIE process as in the vertical current limiter process. Following the DRIE step, the structure was oxidized at 1000 °C using dry O_2 to simultaneously form sharp emitter tips while reducing the pillar diameter. Finally, the thermally grown oxide is removed using 10 : 1 diluted HF. A SEM image of the completed structure is shown in Fig. 9. The pillars are 10 μm tall, with a diameter of 110 nm and a tip radius under 10 nm. Fig. 9 shows a SEM image of the complete FEA structure after field-emission testing. Fig. 10 is a plot of the radii of 209 tips. The statistics follow a log-normal distribution with a mean of 5.6 nm and a standard deviation of 1.3 nm. The tip radius measurements were made using SEM images taken after the device characterization; hence, they are representative of the actual device dimensions.

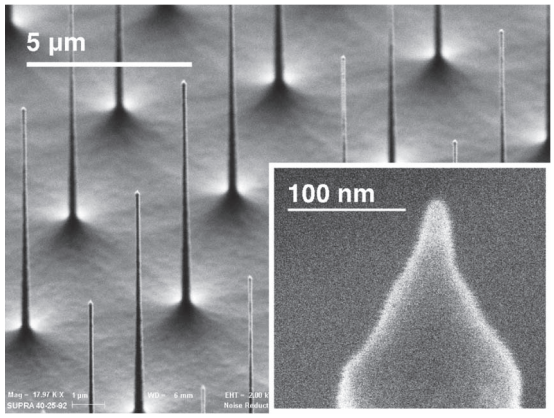

Fig. 9. SEM micrograph of the completed structure. The pillars are 10 μm tall, are 100 nm in diameter, and have an emitter tip radius under 10 nm. (Inset) Detail of a representative emitter tip.

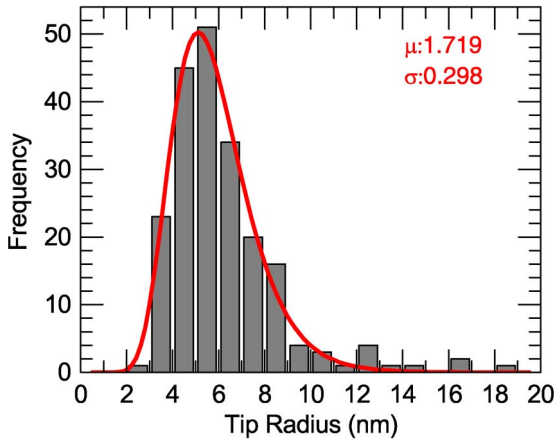

Fig. 10. Radii of 209 field emitters measured using SEM across the die after field-emission testing. The distribution is log normal with a mean of 5.6 nm and a standard deviation of 1.3 nm.

VII. I–V Characterization of FEAs Individually Ballasted by Vertical Current Limiters

Arrays of 1.36 million emitters were fabricated following the process described in Section VI using n-type Si wafers with a nominal donor concentration of 2×10^{14} cm^{-3}. The experimental setup is shown in Fig. 11. A 25 ± 10-μm-thick nylon spacer was used to insulate the emitters from an unaligned perforated extraction grid, resulting in a tip–grid distance of 5–25 μm. When electrons are emitted from the sample, a fraction of the electrons pass through the grid and are collected by a suspended ball-shaped anode biased at +1100 V, allowing us to determine whether the source of the current is leakage through the dielectric spacer or electron field-emission current. The linear relationship between the current collected at the grid and the suspended anode suggests that the origin was field emission. At higher voltages, this linearity does not hold. It is likely that the polymer spacer is beginning to break down at these voltages, resulting in significant leakage current in addition to the field-emission current.

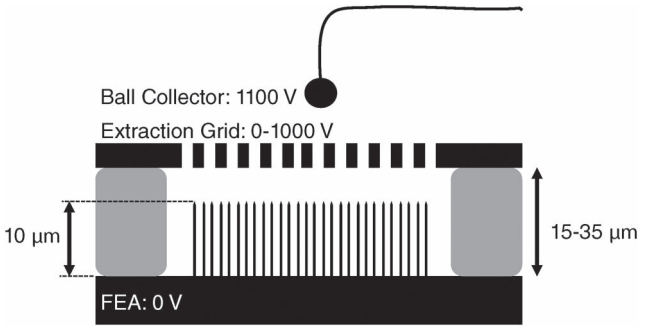

Fig. 11. Schematic of the triode configuration used to test the ballasted FEAs. A nylon polymer gasket acts as a standoff between the FEA and the extraction gate.

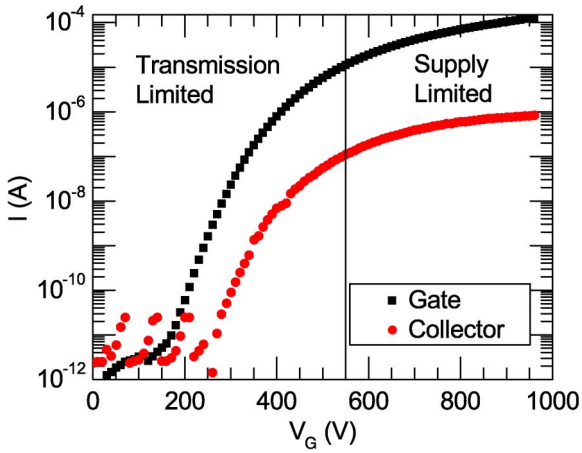

Fig. 12. I–V characteristics for an array of 1.36 million individually ballasted field emitters. At gate voltages over 550 V, the FEA enters a regime where the current is limited by the supply of electrons to the field emitters by the vertical current limiter, rather than the transmission through the barrier.

I–V characterization took place in an ultra-high vacuum testing chamber at a pressure of 9×10^{-10} torr using three commercially available high-voltage source measure units (SMUs) (Keithley model 237 SMUs). Fig. 12 shows the typical I–V characteristics of a 1.36 million tip FEA for electrons collected by both the extraction gate and the anode. The transparency of the extraction gate was about 1%. The Fowler–Nordheim (F–N) plot, shown in Fig. 13, is a common technique for plotting field-emission data. Ideally, there is a linear relationship between the natural log of the current over the square of the gate voltage and the inverse of the gate voltage [19]. At high extraction gate voltages, if the emission current is limited by the vertical current limiters, the F–N plot should deviate from the linear relationship, and the slope should become less negative at higher voltages. At a bias voltage of approximately 600 V, the F–N characteristic in Fig. 13 begins to deviate from its linear characteristics.

The tip radius may be estimated empirically from the slope of the F–N curve $b_{\mathrm{F-N}}$ using

$$\beta = \frac{0.95 \cdot 6.83 \times 10^7 \cdot \phi^{3/2}}{b_{\mathrm{F-N}}} (\mathrm{cm}^{-1}) \tag{2}$$

$$r \approx \frac{1}{\beta} (\mathrm{cm}) \tag{3}$$

where β is the field factor in per centimeters, ϕ is the work function barrier in electronvolts, assumed to be 4.05 eV for

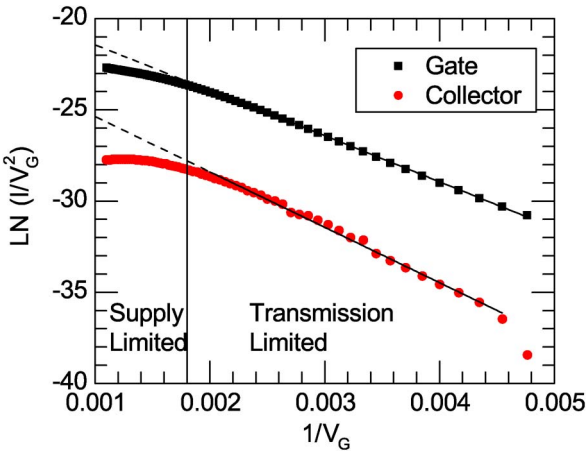

Fig. 13. F–N plot for an array of 1.36 million individually ballasted field emitters, demonstrating the different regions of operation.

n-type Si, and r is the emitter tip radius in centimeters. The slope extracted from the F–N gate current characteristic shown in Fig. 13 was 2942, resulting in a β of 1.80×10^5 cm^{-1} and an r of 55 nm. This result is not consistent with the experimental measured tip radii shown in Fig. 10 and will be examined further hereinafter.

VIII. Discussion

The current–voltage characterization of the individually ballasted FEAs presented in the preceding section is consistent with the results obtained by Velásquez-García *et al.* [13] and the characterization of the vertical current limiter pillars without field-emission structures reported in Section IV. Using the data presented in Table I and assuming that the emission current is limited to 10 pA/emitter, the expected array current is 13.6 μA. From Fig. 13, at a gate-to-source bias voltage of 550 V, we observe the transition of the F–N plot from the regime where the current is limited by the transmission of electrons through the barrier to a supply-limited regime. The corresponding emission from the FEA is 11.1 μA. This result is consistent with our suggestion that the vertical current limiter controls emission current.

We note that the surface of the current limiters reported in Section IV was covered by carefully processed SiO_2, whereas the surface of the current limiters ballasting the FEAs is covered with thin oxides that are not carefully processed and hence may be affected by a higher interface trap density. This increased trap density may have an impact on the saturation current of the current limiters. However, based on the experimentally obtained saturation characteristics of the ballasted FEAs reported earlier, we do not believe that this had a major impact on the ability to use this structure for the ballasting of field-emission arrays.

The tip radius obtained from the F–N plot does not agree well with the tip radius distribution obtained from SEM measurements. The presence of a thin native oxide could manifest itself as a lower field factor, which translates into an implied higher work function. However, assuming a work function increase from 4.05 to 4.5 eV changes the extracted tip radius by less than 20%. Hence, this is not very likely. A better explanation is that

the models that describe the electrostatics of a microfabricated field emitter with a self-aligned gate that is very close to the tip [20], [21] do not translate well to structures where the gate is perforated and located about 25 μm away with tip-to-tip separation of 5 μm and an aspect ratio of 100, as we have in this case. Screening of the tip electrostatic field by proximal tips has been suggested in the literature, particularly when the tip-to-tip distance is far less than the tip-to-gate distance [22].

IX. Conclusion

Arrays of vertical ungated FET current limiters less than 100 nm in diameter with a pitch of 1 μm have been fabricated using batch fabrication techniques. Array sizes from single vertical current limiters to 4M vertical current limiters were characterized. These scaled-down silicon pillars exhibited excellent current control, successfully demonstrating the highest density, smallest diameter, and lowest operating voltage for silicon vertical current limiters ever reported. In addition, field-emission arrays individually ballasted by vertical ungated FET current limiters with 5-μm pitch were fabricated, demonstrating possible current limitation from the current limiters at current levels of 200 μA.

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